## Errata

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## HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that HewlettPackard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

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## Agilent Technologies

# HP 5334B Universal Counter 

CIIL FIRMWARE REV. 1.0
This manual applies to Serial Prefix 2937, unless accompanied by a Manual Change Sheet indicating otherwise

## CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

## WARRANTY

This Hewlett-Packard instrument product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

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The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

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#### Abstract

ASSISTANCE Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.


## SAFETY CONSIDERATIONS

## GENERAL

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.
This product is a Safety Class I instrument (provided with a protective earth terminal).

## BEFORE APPLYING POWER

Verify that the product is set to match the available line voltage and the correct fuse is installed. Refer to Section II, Installation.

## SAFETY EARTH GROUND

An uninterruptible safety earth ground must be provided from the mains power source to the product input wiring terminals or supplied power cable.

## SAFETY SYMBOLS



Alternating current.

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

## SAFETY INFORMATION

## WARNING

Any interruption of the protective grounding conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury. (Grounding one conductor of a two conductor outlet is not sufficient protection.)
Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.
If this instrument is to be energized via an autotransformer (for voltage reduction) make sure the common terminal is connected to the earthed pole terminal (neutral) of the power source.

Instructions for adjustments while covers are removed and for servicing are for use by service-trained personnel only. To avoid dangerous electric shock, do not perform such adjustments or servicing unless qualified to do so.

For continued protection against fire, replace the line fuse(s) only with 250 V fuse(s) of the same current rating and type (for example, normal blow, time delayi. Do not use repaired fuses or short circuited fuseholders.

When measuring power line signals, be extremely careful and always use a step-down isolation transformer whose output voltage is compatible with the input measurement capabilities of this product. This product's front and rear panels are typically at earth ground, so NEVER TRY TO MEASURE AC POWER LINE SIGNALS WITHOUT AN ISOLATION TRANSFORMER.

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## SECTION 4 PERFORMANCE TESTS

## 4-1. INTRODUCTION

4-2. The procedures in this section provide three groups of tests to check for proper operation of the HP 5334B Universal Counter. The first is a quick method of verifying the basic functioning of the counter when its normal operation is in question. The second is a complete test of the instrument's electrical performance using the specifications of Table 1-1 as the performance standards. And the third is an HP-IB verification test using either the HP 9000 Series $200 / 300$ computer or the HP 85A computer as a controller. All tests can be performed without access to the interior of the instrument.

## 4-3. EQUIPMENT REQUIRED

4-4. Equipment required for the performance tests is listed in Table 1-4, Recommended Test Equipment. Any equipment that satisfies the critical specifications given in the table may be substituted for the recommended model(s).

## 4-5. OPERATIONAL VERIFICATION/PERFORMANCE TEST RECORD

4-6. Results of the operation verification tests may be recorded on a copy of the Operational Verification Test Record which follows the verification tests, Table 4-1. The results of the complete performance tests may be recorded on a copy of the Performance Test Record which follows the performance tests, Table 4-2.

## 4-7. CALIBRATION CYCLE

4-8. To maintain the HP 5334B in optimum operating condition, depending on the use and environmental conditions, it is suggested that the instrument be checked using the performance tests at least once each year. The Counter's reference oscillator must be checked and adjusted, if necessary, to a house frequency standard before beginning the performance tests. Refer to Adjustment Procedure 5-15 in Section V of this manual. Follow the preliminary instructions given in the INTRODUCTION and SAFETY CONSIDERATIONS paragraphs in Section V.

4-9. Additionally, to maintain peak instrument performance between yearly checks, the instruments containing the standard time base crystal oscillator, i.e., all non-Option 010 units, should be adjusted every 3 months to a house frequency standard using Adjustment Procedure 5-15, Reference Oscillator Adjustment in Section V of this manual. Again, refer to the preliminary instructions before beginning the adjustment procedure.

## 4-10. TEST PROCEDURES

4-11. It is assumed that the person performing the following tests understands how to operate the specified test equipment. Equipment settings, other than those for the Universal Counter, are stated in general terms. It is also assumed that the person performing the tests will supply whatever cables, connectors, and adapters that are necessary.

## 4-12. OPERATIONAL VERIFICATION TESTS

4-13. The tests included here are not as thorough and exhaustive as the performance tests. This group of tests is intended only to serve as a method for giving the operator a high degree of confidence that the instrument is performing properly. No attempt is made to check the specifications of the instrument.

4-14. These tests are useful for incoming QA or as a first check on an instrument suspected of having a problem.

## 4-15. Preliminary Procedure

## CAUTION

Before the Universal Counter is switched on, it must be set to the same line voltage as the power source or damage to the instrument may result. For details, see Power Requirements, Line Voltage Selection, Power Cable, and associated warnings and cautions in Section II of the Operating and Programming Manual.

## NOTE

To avoid confusion, each test procedure begins with a REINITIALIZATION of the instrument. This simply means switching the HP 5334B to STANDBY and then to ON .

Procedure:

1. Set the HP 5334B as follows:

POWER ............................................................................................................................
TIME BASE............................................................................................INT (rear panel)
2. Connect the HP 5334B as follows:

HP 5334B Power Cable
to Line Voltage
Observe: STANDBY LED is ON.
3. Do not connect an input signal to the HP 5334B.

## 4-16. POWER-UP SELF-TEST/DIAGNOSTIC MODE

Description: During the power-up sequence, the HP 5334B performs a fairly thorough check of major components.

## Procedure:

1. Set the HP 5334B as follows:

POWER

Observe: STANDBY LED goes out.
2. All front panel LEDs light momentarily (except STANDBY LED which does not light and ARM and GATE annunciators which flash alternately).
3. The instrument's model number, "HP 5334b", is displayed.
4. The instrument's HP-IB address is displayed. (Address " 03 " is set at the factory but can be set by the user to addresses " 00 " to " 30 ").
5. If the instrument successfully executes the power-up self-test routine, the front panel displays "PASS" and then defaults to preset conditions.

## Front Panel Preset Conditions:

$\qquad$



AUTO TRIG...........................................................................................ON
Channel A and B TRIGGER LEVEL LEDs.............................................Flash Alternately
All Other Indicators................................................................................OFF
Test Record: Mark Pass or Fail on the Operational Verification Test Record Card, line 1.

## What Checked:

1. The three microcomputers perform a ROM and RAM check.
2. The alternately flashing ARM and GATE annunciators indicate that the Measurement microcomputer passes the ROM/RAM test.
3. The Executive microcomputer runs the front panel display check.
4. The Executive and Measurement microcomputers perform a limited Input/Output port check.
5. The Measurement microcomputer checks for the presence of a time base oscillator.
6. A test of the Multiple-Register Counter (MRC) is made to check for basic operation.
7. A handshake communication test is performed between the Executive and Measurement and the Executive and HP-IB microcomputers.
8. The Executive microcomputer reads the HP-IB address from the CMOS RAM and displays it to the front panel.

For Failures: Any failures during the power-up cycle will disable the counter and produce a display of a numbered Error or Fail message. For a description of failure messages, refer to Error Indications in Section III of the Operating and Programming Manual.

Additional Comments: The HP 5334B can be put into a diagnostic mode where it repeatedly cycles through the power-up self tests. This is accomplished by pressing the RESET/LOCAL key while switching the power ON. The tests are repeated until the power is switched to STANDBY.

## NOTE

In the diagnostic mode, neither the instrument model number nor the HP-IB address is displayed.

## 4-17. READ LEVELS

Description: Checking the operation of the READ LEVELS function can indicate the health of several circuits critical to the operation of the counter.

## Procedure:

1. Set the HP 5334B as follows:

Reinitialize the 5334B.
No Input Signal.
READ LEVELS. Trigger Levels
(Press once to display trigger level settings, indicated on the display by an " L " in the place of the exponent value.)
2. Rotate each front panel TRIGGER LEVEL/SENS control fully counterclockwise, then fully clockwise.

Observe: The voltage extremes displayed should be less than -5 V and greater than +5 V , respectively.
3. From the fully clockwise position, slowly rotate each control counterclockwise, then clockwise past the midpoint position where the displayed voltage is approximately 0 V .

Observe: Each trigger light should turn on then off as the polarity level changes between +100 mV and -100 mV .
4. Adjust each control for a setting of +2.54 V , and then -2.54 V .

Observe: These exact settings should be possible with the voltage reading increasing or decreasing in 0.02 V steps.
5. Set the HP 5334B as follows:

SENS. ON

Observe: Both trigger level settings should display 0.00 V .
Test Record: Mark Pass or Fail on the Operational Verification Test Record Card, line 2.

## What checked:

1. In the READ LEVELS mode, the Digital-to-Analog circuitry and the Measurement microcomputer are operating while the Input Amplifier and Multiple-Register Counter circuitry are inactive.
2. The DAC circuitry and the Measurement Data Bus are operating properly if the $\pm 2.54 \mathrm{~V}$ settings can be obtained.
3. If all tests are passed, the likelihood is high that the DACs, operational amplifier loops, the Read Level comparators, the analog switches (all are DAC circuitry components), and the front panel pots are operating properly.

For Failures: If any failures are encountered in this test, refer to Section VIII of this manual. The Digital-toAnalog Block is a likely candidate as a starting point for troubleshooting. Other circuit blocks involved are the Measurement, Executive, and Front Panel blocks.

## 4-18. RATIO A/B

Description: This test uses the time base oscillator to drive the A and B input amplifier in a test of the MultipleRegister Counter (MRC).

## Procedure:

1. Connect the rear panel TIME BASE oscillator signal to the Channel A Input.
2. Set the HP 5334B as follows:
```
Reinitialize the 5334B.
COM A.......................................................................................................ON
AUTO TRIG..............................................................................................OFF
TRIGGER LEVEL controls .....................................................................midpoint setting
CHAN A and B 50\Omega..................................................................................ON
GATE TIME.................................................................................................... }1\mathrm{ Second
FUNCTION................................................................................................RATIO A/B
```

Observe: The HP 5334B front panel displays $10000000 \mathrm{MHz} \pm 0.2 \mathrm{~Hz}$ and both trigger lights are flashing.
Test Record: Mark Pass or Fail on the Operational Verification Test Record Card, line 3.

## What Checked:

1. The operation of the MRC is checked using the ratio function.
2. The 10 MHz oscillator signal at the rear panel BNC connector is verified.

For Failure: Refer to Section VIII of this manual. The Measurement Block contains the MRC (MultipleRegister Counter) and other blocks involved are the Input Amplifier, Executive, Front Panel, and Time Base/Power Supply blocks.

## 4-19. FREQUENCY

Description: Using this test, a frequency is measured which will exercise the interpolators.

## Procedure:

1. Connect the rear panel TIME BASE oscillator signal to the Channel A Input.
2. Set the HP 5334B as follows:

Reinitialize the 5334B.
Observe: The HP 5334B front panel displays $10.0000000 \mathrm{MHz} \pm 0.2 \mathrm{~Hz}$.
Test Record: Mark Pass or Fail on the Operational Verification Test Record Card, line 4.
What Checked: The interpolators which provide the accuracy of the frequency count are tested. Defective interpolators may cause the reading to vary up to $\pm 100 \mathrm{~Hz}$.

For Failure: Refer to Section VIII of this manual. The interpolators are part of the Measurement Block. Other blocks involved here are the Input Amplifier, DAC, Executive, Front Panel, and Time Base/Power Supply blocks.

## 4-20. INPUT SIGNAL CONDITIONING CHECK

Description: This series of checks performs a functional test of the front panel relays and circuitry associated with those relays.

## Procedure:

1. Connect the rear panel TIME BASE oscillator signal to the Channel A Input.
2. Set the HP 5334B as follows:
```
Reinitialize the 5334B.
AUTO TRIG..............................................................................................OFF
COM A.......................................................................................................ON
CHAN A and B 50\Omega .................................................................................ON
GATE TIME.................................................................................................... Second
```

3. Adjust both TRIGGER LEVEL/SENS controls clockwise until trigger lights just go off.
4. Set the HP 5334B as follows:
COM A. ..... OFF
CHAN A and B $50 \Omega$ ..... OFF
Observe: The HP 5334B front panel displays $10.0000000 \mathrm{MHz} \pm 0.2 \mathrm{~Hz}$. Channel A trigger light flashing and Channel B light not flashing.
5. Set the HP 5334B as follows:
CHAN A $50 \Omega$ ..... ON
Observe: The HP 5334B front panel displays all dashes and Channel A trigger light stops flashing.
6. Set:
CHAN A $50 \Omega$ ..... OFF
Observe: Condition prior to switching in $50 \Omega$ impedance.
7. Set:
CHAN A X10 ATTN ..... ON
Observe: The HP 5334B front panel displays all dashes and Channel A trigger light stops flashing.
8. Set:
CHAN A X10 ATTN ..... OFF
Observe: Condition prior to switching in X10 attenuator.
9. Set:
100 kHz FILTER A ..... ON
Observe: The HP 5334B front panel displays all dashes and Channel A trigger light stops flashing.
10. Set:
100 kHz FILTER A. ..... OFF
Observe: Condition prior to switching in 100 kHz Filter.
11. Set:
COM A. ..... ON
FUNCTION ..... FREQ B
Connect the rear panel TIME BASE oscillator signal to the Channel B Input.
Observe: The HP 5334B front panel stops updating and the trigger lights stop flashing.
12. Set:
COM A
OFF
Observe: The HP 5334B front panel displays $10.0000000 \mathrm{MHz} \pm 0.2 \mathrm{~Hz}$. Channel B trigger light flashing and Channel A trigger light not flashing.
13. Set:
$\qquad$CHAN B $50 \Omega$ON
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Observe: The HP 5334B front panel displays all dashes and Channel B trigger light stops flashing.
14. Set:

CHAN B $50 \Omega$.
OFF
Observe: Condition prior to switching in $50 \Omega$ impedance.
15. Set:

CHAN B X10 ATTN
ON
Observe: The HP 5334B front panel displays all dashes and Channel B trigger light stops flashing.
16. Set:

CHAN B X10 ATTN
OFF
Observe: Condition prior to switching in X10 ATTN.
Test Record: Mark Pass or Fail on the Operational Verification Test Record Card, line 5.
What Checked: Relays and circuitry.
For Failures: Refer to Section VIII of this manual. The Input Amplifier and Executive Blocks are the main components of this test. Other blocks involved are DAC, Measurement, and Front Panel blocks.

## 4-21. T.I. $A \rightarrow B$

Description: Slope switch verification.

## Procedure:

1. Connect the rear panel TIME BASE oscillator signal to the Channel A Input.
2. Set the HP 5334B as follows:

Reinitialize the 5334B.
COM A.................................................................................................................ON
TRIGGER LEVEL controls .............................................................................set to $0 \mathrm{~V} \pm 0.2 \mathrm{~V}$
AUTO TRIG using READ LEVELS "L" mode

CHAN A and B $50 \Omega$..........................................................................................ON
GATE TIME....................................................................................................... 1 Second
FUNCTION.......................................................................................................T.I. A $\rightarrow$ B
Observe: The HP 5334B front panel displays $0 \mathrm{~ns} \pm 6 \mathrm{~ns}$.
3. Set both:

Channel A and B Negative SLOPE
ON
(Counter now triggers on negative slope.)
Observe: The HP 5334B front panel displays $0 \mathrm{~ns} \pm 6 \mathrm{~ns}$.
4. Set:

> Channel A to Negative SLOPE ................................................................................................................................................ Channel B to Negative SLOPE

Observe: The HP 5334B front panel displays $50 \mathrm{~ns} \pm 6 \mathrm{~ns}$.
5. Set:

Channel A to Negative SLOPE.........................................................................ON
Channel B to Negative SLOPE ........................................................................OFF
Observe: The HP 5334B front panel displays $50 \mathrm{~ns} \pm 6 \mathrm{~ns}$.
Test Record: Mark Pass or Fail on the Operational Verification Test Record Card, line 6.
What Checked: Time interval measurement and slope switch operation.
For Failures: Refer to Section VIII of this manual. In this case, the Input Amplifier, DAC, Measurement, Executive, Front Panel, and Time Base/Power Supply blocks are involved.

## 4-22. AUTO TRIGGER

Description: The Measurement microcomputer sends a signal to the DAC block and disables the front panel trigger level controls.

## Procedure:

1. Connect the rear panel TIME BASE oscillator signal to the Channel A Input.
2. Set the HP 5334B as follows:
```
Reinitialize the 5334B.
GATE TIME............................................................................................... 1 Second
```

Observe: The HP 5334B front panel displays $10.0000000 \mathrm{MHz} \pm 0.2 \mathrm{~Hz}$ and both Channel A and B trigger lights are flashing.
3. Rotate Channel A trigger level control.

Observe: There is no effect on the Counter's operation.
4. Set AUTO TRIG to OFF. Rotate Channel A trigger level control.

Observe: Extreme clockwise and counterclockwise control settings will stop the gating and update of the Counter. Trigger light stops flashing.
5. Set AUTO TRIG to ON. Connect the rear panel TIME BASE oscillator signal to Input B. Set FUNCTION to FREQ B.

Observe: The HP 5334B front panel displays $10.0000000 \mathrm{MHz} \pm 0.2 \mathrm{~Hz}$ and Channel A and B trigger lights are flashing.
6. Rotate Channel B trigger level control.

Observe: There is no effect on the Counter's operation.
7. Set AUTO TRIG to OFF. Rotate Channel B trigger level control.

Observe: Extreme clockwise and counterclockwise control settings will stop the gating and update of the Counter. Trigger light stops flashing.

Test Record: Mark Pass or Fail on the Operational Verification Test Record Card, line 7.
What Checked: Control lines and DAC circuitry.
For Failures: Refer to Section VIII of this manual. The test involves all of the functional blocks: the Input Amplifier, DAC, Measurement, Executive, Front Panel, and Time Base/Power Supply blocks.

## 4-23. CHANNEL C (Option 030)

This operational check is for HP 5334B's containing Option 030.
Description: The Channel C option is checked by simply measuring a frequency within its range of 90 MHz to 1300 MHz .

Equipment: A signal source capable of outputting some frequency from 90 MHz to 1300 MHz .

## Procedure:

1. Set the signal source as follows:
Frequency.
.90 to 1300 MHz
Amplitude
300 mV rms $(+2.5 \mathrm{dBm})$
2. Set the HP 5334B as follows:

Reinitialize the 5334B. FUNCTION. FREQ C
3. Connect the signal source to the HP 5334B Input C.
4. Adjust the Channel C Sensitivity control as needed to cause the Counter to gate and display a stable reading. Observe: The HP 5334B front panel displays the generated frequency.

Test Record: Mark Pass or Fail on the Operational Verification Test Record Card, line 11.
What Checked: Basic operation of the Channel C option.
For Failures: Refer to Section VIII of this manual. The Channel C, Measurement, Executive, and Front Panel blocks are involved here.

Table 4-1. HP 5334B Operational Verification Test Record


## 4-24. PERFORMANCE TESTS

4-25. The following procedures test the electrical performance of the HP 5334B Universal Counter using the specifications in Table 1-1 as the performance standards. The tests included here are much more specific and rigorous than the operational verification procedures. Use these procedures to ensure that the instrument in question is operating at its highest level at incoming QA, the annual calibration cycle check, or following any of the adjustment procedures.

4-26. The procedures were designed to be performed sequentially in order to fully test the HP 5334B.

## NOTE

If the performance tests are to be considered valid, the the following conditions must be met:
a. The Universal Counter must have a 30 -minute warmup.
b. The reference oscillator must be set to a frequency standard. Perform the Reference Oscillator Frequency Adjustment before beginning these tests. This is adjustment 5-15 in Section V, ADJUSTMENTS, of this manual.

## NOTE

The $\pm$ resolution limits specified in the following procedures assume that the test equipment being used is calibrated and operating at its performance limits. When this is not the case, problems can occur. For example, noise on an input signal to the Counter will result in the display of what seems to be an inaccurate measurement. This condition must be considered when observed measurements do not agree with the performance test limits

## 4-27. Preliminary Procedure

## CAUTION

Before the Universal Counter is switched on, it must be set to the same line voltage as the power source or damage to the instrument may result. For details, see Power Requirements, Line Voltage Selection, Power Cable, and associated warnings and cautions in Section II of the Operating and Programming Manual.

## NOTE

To avoid confusion, each test procedure begins with a REINITIALIZATION of the instrument. This simply means switching the HP 5334B to STANDBY and then to ON .

## Procedure:

1. Set the HP 5334B as follows:

POWER
STANDBY
TIME BASE.............................................................................................INT (rear panel)
2. Connect the HP 5334B as follows:

5334B Power Cable $\qquad$ to Line Voltage

Observe: STANDBY LED is ON.
3. The HP 5334B Time Base oscillator is used as the reference for the other instruments in these tests.

Connect the HP 5334B rear panel TIME BASE signal to both the function generator and the signal generator. Set these instruments to operate on the external time base from the HP 5334B. Figure 4-1.


Figure 4-1. Time Base Reference Setup

## 4-28. CHANNEL A FREQUENCY RESPONSE AND SENSITIVITY TEST, $10 \mathrm{~Hz}-20 \mathrm{MHz}$

Specification: Refer to Table 1-1, HP Model 5334B Specifications, for Frequency Response and Sensitivity specifications.

Description: The frequency measuring range of the Counter is tested at minimum sensitivity specifications and four different frequency settings.

Frequencies and conditions tested:
10 Hz and 20 MHz , dc coupled, $1 \mathrm{M} \Omega$
30 Hz and 20 MHz , ac coupled, $1 \mathrm{M} \Omega$
1 MHz and 20 MHz , ac coupled, $50 \Omega$


Figure 4-2. Channel A Frequency and Sensitivity Setup, $10 \mathrm{~Hz}-20 \mathrm{MHz}$

## Equipment:

Function Generator
HP 3325A

## Procedure:

1. Set the function generator as follows:
Frequency.
10 Hz
Amplitude
15 mV rms
Function
Sine Wave
2. Set the HP 5334B as follows:
Reinitialize the 5334B.
FUNCTION.
.FREQ A
SENS....................................................................................................................ON
CHAN A TRIG/SENS control...........................................................................fully CW
3. Connect the function generator signal to the HP 5334B Input A using a $50 \Omega$ feedthrough connector as shown in Figure 42.
VERIFY: The Counter displays $10 \mathrm{~Hz} \pm 0.03 \mathrm{~Hz}$.
4. Record the measurement on the Performance Test Record Card, line 1.
5. Set the function generator as follows:
Frequency.
20 MHz
VERIFY: The Counter displays $20 \mathrm{MHz} \pm 0.3 \mathrm{~Hz}$.
6. Record the measurement on the Performance Test Record Card, line 2.
7. Set the function generator as follows:
Frequency 30 Hz
8. Set the HP 5334B as follows:
AC.
.ON
VERIFY: The Counter displays $30 \mathrm{~Hz} \pm 0.03 \mathrm{~Hz}$.
9. Record the measurement on the Performance Test Record Card, line 3.
10. Set the function generator as follows:
Frequency
.20 MHz
VERIFY: The Counter displays $20 \mathrm{MHz} \pm 0.3 \mathrm{~Hz}$
11. Record the measurement on the Performance Test Record Card, line 4.
12. Set the function generator as follows:
Frequency
1 MHz

## NOTE

Remove the $50 \Omega$ feedthrough connector.
13. Set the HP 5334B as follows:
$50 \Omega$
ON
VERIFY: The Counter displays $1 \mathrm{MHz} \pm 0.04 \mathrm{~Hz}$.
14. Record the measurement on the Performance Test Record Card, line 5.
15. Set the function generator as follows:

Frequency
20 MHz
VERIFY: The Counter displays $20 \mathrm{MHz} \pm 0.3 \mathrm{~Hz}$.
16. Record the measurement on the Performance Test Record Card, line 6.

Failure: If any of these tests fail, refer to Section V, Adjustments, paragraphs 5-16 and 5-18 as a first step in troubleshooting.

## 4-29. CHANNEL B FREQUENCY RESPONSE AND SENSITIVITY TEST, $10 \mathrm{~Hz}-20 \mathrm{MHz}$

Specification: Refer to Table 1-1; HP Model 5334B Specifications, for Frequency Response and Sensitivity specifications.

Description: The frequency measuring range of the Counter is tested at minimum sensitivity specifications and four different frequency settings.

Frequencies and conditions tested:
10 Hz and 20 MHz , dc coupled, $1 \mathrm{M} \Omega$
30 Hz and 20 MHz , ac coupled, $1 \mathrm{M} \Omega$
1 MHz and 20 MHz , ac coupled, $50 \Omega$


Figure 4-3. Channel B Frequency and Sensitivity Setup, $10 \mathrm{~Hz}-20 \mathrm{MHz}$

## Equipment:

Function Generator

## Procedure:

1. Set the function generator as follows:
Frequency
10 Hz

Amplitude ................................................................................................................... 15 V rms
Function Sine Wave
2. Set the HP 5334B as follows:

Reinitialize the 5334B.
FUNCTION.
FREQ B
SENS
ON
CHAN B TRIG/SENS control fully CW
3. Connect the function generator signal to the HP 5334B Input B using a 50 Ohm feedthrough connector as shown in Figure 4-3.
4. Repeat the tests of paragraph $4-31$ for Channel B and record the measurements on the Performance Test Record Card, lines 7 through 12 . Begin the tests at the verification of 10 Hz in paragraph $4-31$, step 4.

Failure: If any of these tests fail, refer to Section V, Adjustments, paragraphs 5-17 and 5-19 as a first step in troubleshooting.

## 4-30. CHANNEL A FREQUENCY RESPONSE AND SENSITIVITY TEST, $80 \mathrm{MHz}-100 \mathrm{MHz}$

This test is for instruments that do not contain the Option 060 Rear Panel Inputs, i.e., instruments with Front Inputs only.

Specification: Refer to Table 1-I, HP Model 5334B Specifications, for Frequency Response and Sensitivity specifications.

Description: The frequency measuring range of the Counter is tested at minimum sensitivity specifications and two different frequency settings.

## Frequencies and conditions tested:

80 MHz and 100 MHz , dc coupled, $1 \mathrm{M} \Omega$
80 MHz and 100 MHz , ac coupled, $1 \mathrm{M} \Omega$
80 MHz and 100 MHz , ac coupled, $50 \Omega$


Figure 4-4. Channel A Frequency and Sensitivity Setup, $80 \mathrm{MHz}-100 \mathrm{MHz}$

## Equipment:

Signal Generator
HP 8660A/C

Procedure:

1. Set the signal generator as follows:
Frequency
80 MHz
Amplitude
35 mV ms
2. Set the HP 5334B as follows:
Reinitialize the 5334B.
FUNCTION.
FREQ A
SENS.
ON
CHAN A TRIG/SENS control fully CW
3. Connect the signal generator to the HP 5334B Input A using a $50 \Omega$ feedthrough connector as shown in Figure 4-4.

VERIFY: The Counter displays $80 \mathrm{MHz} \pm 2 \mathrm{~Hz}$.
4. Record the measurement on the Performance Test Record Card, line 13.
5. Set the signal generator as follows:
Frequency
100 MHz
Amplitude
.35 mV rms

VERIFY: The Counter displays $100 \mathrm{MHz} \pm 2 \mathrm{~Hz}$.
6. Record the measurement on the Performance Test Record Card, line 14.
7. Set the signal generator as follows:
Frequency..................................................................................................................................................................................................... 35 mV rms
Amplitude
8. Set the HP 5334B as follows:

AC.
ON

VERIFY: The Counter displays $80 \mathrm{MHz} \pm 2 \mathrm{~Hz}$.
9. Record the measurement on the Performance Test Record Card, line 15.
10. Set the signal generator as follows:

Frequency.
100 MHz
Amplitude ............................................................................................................. 35 mV rms
VERIFY: The Counter displays $100 \mathrm{MHz} \pm 2 \mathrm{~Hz}$.
11. Record the measurement on the Performance Test Record Card, line 16.
12. Set the signal generator as follows:

Frequency............................................................................................................. 80 MHz
Amplitude ............................................................................................................. 35 mV rms

## NOTE

Remove the $50 \Omega$ feedthrough connector.
13. Set the HP 5334B as follows:
$\qquad$
VERIFY: The Counter displays $80 \mathrm{MHz} \pm 2 \mathrm{~Hz}$.
14. Record the measurement on the Performance Test Record Card, line 17.
15. Set the signal generator as follows:

Frequency.
100 MHz
Amplitude 35 mV rms

VERIFY: The Counter displays $100 \mathrm{MHz} \pm 2 \mathrm{~Hz}$.
16. Record the measurement on the Performance Test Record Card, line 18.

Failure: If any of these tests fail, refer to Section V, Adjustments, paragraphs 5-16 and 5-18 as a first step in troubleshooting.

## 4-31. CHANNEL B FREQUENCY RESPONSE AND SENSITIVITY TEST, $80 \mathrm{MHz}-100 \mathrm{MHz}$

This test is for instruments that do not contain Option 060 Rear Panel Inputs, i.e., instrument with Front Inputs only.

Specification: Refer to Table 1-1, HP Model 5334B Specifications, for Frequency Response and Sensitivity specifications.

Description: The frequency measuring range of the Counter is tested at minimum sensitivity specifications and two different frequency settings.

Frequencies and conditions tested:
80 MHz and 100 MHz , dc coupled, $1 \mathrm{M} \Omega$
80 MHz and 100 MHz , ac coupled, $1 \mathrm{M} \Omega$
80 MHz and 100 MHz , ac coupled, $50 \Omega$
 $80 \mathrm{MHz}-100 \mathrm{MHz}$

## Equipment:

Signal Generator $\qquad$ HP 8660A/C

## Procedure:

1. Set the signal generator as follows:
$\qquad$Amplitude35 mV ms
2. Set the HP 5334B as follows:
Reinitialize the 5334B.
FUNCTION
FREQ B
SENS ON
CHAN B TRIG/SENS control fully CW
3. Connect the signal generator to the HP 5334B Input B using a $50 \Omega$ feedthrough connector as shown in Figure 4.5.
4. Repeat the tests of paragraph $4-33$ for Channel $\mathbf{B}$ and record the measurements on the Performance Test Record Card, lines 19 through 24. Begin the tests at the verification of 80 MHz in paragraph $4-33$, step 4 .

Failure: If any of these tests fail, refer to Section V, Adjustments, paragraphs 5-17 and 5-19 as a first step in troubleshooting.

## 4-32. CHANNEL A FREQUENCY RESPONSE AND SENSITIVITY TEST, $80 \mathrm{MHz}-100 \mathrm{MHz}$

This test is for instrument that contain the Option 060 Rear Panel Inputs, i.e., instruments with both Front and Rear Inputs.

Specification: Refer to Table 1-1, HP Model 5334B Specifications, for Option 060 Frequency Response and Sensitivity specifications.

Description: The frequency measuring range of the Counter is tested at minimum sensitivity specifications and two different frequency settings.

Frequencies and conditions tested:
80 MHz and 100 MHz , dc coupled, $1 \mathrm{M} \Omega$
80 MHz and 100 MHz , ac coupled, $1 \mathrm{M} \Omega$


Figure 4-6. Channel A Frequency and Sensitivity Setup for Option 060

## Procedure:

## 1. Set the signal generator as follows:

Frequency.................................................................................................................................................................................................................
Amplitud
2. Set the HP 5334B as follows:
Reinitialize the 5334B. FUNCTION. ..... FREQ A
SENS ..... ON
CHAN A TRIG/SENS control ..... fully CW
3. Connect $50 \Omega$ feedthroughs or terminations on the rear panel A and B Inputs.
4. Connect the signal generator to the HP 5334B front panel Input A as shown in Figure 4-6.
VERIFY: The Counter displays $80 \mathrm{MHz} \pm 2 \mathrm{~Hz}$.
5. Record the measurement on the Performance Test Record Card, line 25.
6. Set the signal generator as follows:
Frequency ..... 100 MHz
Amplitude ..... 50 mV rms
VERIFY: The Counter displays $100 \mathrm{MHz} \pm 2 \mathrm{~Hz}$.
7. Record the measurement on the Performance Test Record Card, line 26.
8. Set the signal generator as follows: ..... 80 MHz
Amplitude ..... 50 mV rms
9. Set the HP 5334B as follows:
AC. ..... ON
VERIFY: The Counter displays $80 \mathrm{MHz} \pm 2 \mathrm{~Hz}$.
10. Record the measurement on the Performance Test Record Card, line 27.
11. Set the signal generator as follows:
Frequency100 MHz
Amplitude ..... 50 mV rms
VERIFY: The Counter displays $100 \mathrm{MHz} \pm 2 \mathrm{~Hz}$.
12. Record the measurement on the Performance Test Record Card, line 28.

Failure: If any of these tests fail, refer to Section V, Adjustments, paragraphs 5-16 and 5-18 as a first step in troubleshooting.

## 4-33. CHANNEL B FREQUENCY RESPONSE AND SENSITIVITY TEST, $80 \mathrm{MHz}-100 \mathrm{MHz}$

This test is for instruments that contain the Option 060, i.e., instruments with both Front and Rear Inputs.
Specification: Refer to Table 1-1, HP Model 5334B Specifications, for Option 060 Frequency Response and Sensitivity specifications.

Description: The frequency measuring range of the Counter is tested at minimum sensitivity specifications and two different frequency settings.

Frequencies and conditions tested:
80 MHz and 100 MHz , dc coupled, $1 \mathrm{M} \Omega$ 80 MHz and 100 MHz , ac coupled, $1 \mathrm{M} \Omega$


Figure 4-7. Channel B Frequency and Sensitivity Setup for Option 060

Equipment:
Signal Generator
HP 8660A/C

Procedure:

1. Set the signal generator as follows:

Frequency.
80 MHz
Amplitude
.50 mV rms
2. Set the HP 5334B as follows:
Reinitialize the 5334B.
FUNCTION. FREQ B
SENS ON
CHAN B TRIG/SENS control fully CW
3. Connect $50 \Omega$ feedthroughs or terminations on the rear panel $A$ and $B$ Inputs.
4. Connect the signal generator to the HP 5334B front panel Input B as shown in Figure 4-7.
5. Repeat the tests of paragraph $4-35$ for Channel B and record the measurements on the Performance Test Record Card, lines 29 through 32. Begin the tests at the verification of 80 MHz in paragraph 4-35, step 5 .

Failures: If any of these tests fail, refer to Section V, Adjustments, paragraph 5-17 and 5-19 as a first step in troubleshooting.

## 4-34. PERIOD A TEST

Specification: Refer to Table 1-1, HP Model 5334B Specifications, for Period A specifications.
Description: The minimum specified period measurement of 10 ns is verified using a 100 MHz input signal.


Figure 4-8. Period A Test Setup

## Equipment:

Signal Generator
.HP 8660A/C

## Procedure:

1. Set the signal generator as follows:

Frequency.......................................................................................................................................................................................................................
Amplitude

## NOTE

## OPTION 060

If the HP 5334B has Option 060 (rear panel inputs), terminate the unused Channel A input (front or rear) with a $50 \Omega$ load.
2. Set the HP 5334B as follows:

Reinitialize the 5334B.
FUNCTION.........................................................................................................................
GATE TIME............................................................................................ 1 Second

CHAN A TRIG/SENS control..........................................................................
3. Connect the signal generator output to the HP 5334B Input A using a 50 Ohm feedthrough connector as shown in Figure 4-8.

## NOTE

Do not use a $50 \Omega$ feedthrough connector at the Input for Counters with Option 060.

VERIFY: The Counter displays $10 \mathrm{~ns} \pm .0000001 \mathrm{~ns}$.
4. Record the Period A measurement on the Performance Test Record Card, line 33.

Failure: If the instrument under test does not meet the test specification, consider performing the adjustments in Section V of this manual as a first step in correcting the problem.

## 4-35. PULSE WIDTH A TEST

Specification: Refer to Table 1-1, HP Model 5334B Specifications, for Pulse Width A specifications.

Description: A pulse width is generated and then measured with the HP 5334B to verify the Counter's performance.


TSE日_L2
Figure 49. Pulse Width A Test Setup

## Equipment:

Signal Generator
HP 8660A/C

## Procedure:

1. Set the signal generator as follows:
Frequency
100 MHz
Amplitude
200 mV rms
2. Set the HP 5334B as follows:

Reinitialize the 5334B. FUNCTION

PULSE WIDTH A

## NOTE

## OPTION 060

If the HP 5334B has Option 060 (rear panel inputs), terminate the unused Channel A input (front or rear) with a $50 \Omega$ load.
3. Connect the signal generator output to the HP 5334B Input A using a $50 \Omega$ feedthrough connector as shown in Figure 4-9.

## NOTE

Do not use a $50 \Omega$ feedthrough connector at the Input for Counters with Option 060.

VERIFY: The Counter displays $5 \mathrm{~ns} \pm 4 \mathrm{~ns}$.
4. Record the pulse width measurement on the Performance Test Record Card, line 34.

Failure: If the instrument under test does not meet the test specification, consider performing the adjustments in Section V of the Service manual as a first step in correcting the problem.

## 4-36. TIME INTERVAL A TO B TEST

Specification: Refer to Table 1-1, HP Model 5334B Specifications, for Time Interval A to B specification.
Description: Time Interval measuring accuracy is verified using a known generated signal.


Figure 4-10. Time Interval $\bar{A}$ to $\bar{B}$ Test Setup

## Equipment:

$\qquad$

## Procedure:

1. Set the function generator as follows:
Frequency 5 MHz
Amplitude 200 mV p-p
Function
Square Wave
2. Set the HP 5334B as follows:

Reinitialize the 5334B.
FUNCTION.........................................................................................................T.I. A $\rightarrow$ B
COM A.
ON
100 GATE AVERAGE....................................................................................ON
SENS.......................................................................................................... ON
A \& B TRIG/SENS controls.......................................................................................... 1 CW
CHAN A and B 50』......................................................................................... ON
CHAN B Negative SLOPE ............................................................................... ON (falling edge)
3. Connect the function generator output to the HP 5334B Input A.

VERIFY: The Counter displays $100 \mathrm{~ns} \pm 6$ ns.
4. Record the Time Interval measurement on the Performance Test Record, line 35.

Failure: If the instrument under test does not meet the test specification, consider performing the adjustments in Section V of this manual as a first step in correcting the problem.

## 4-37. TIME INTERVAL A TO B DELAY TEST

Specification: Refer to Table 1-1, HP Model 5334B Specifications, for T.I. A to B Delay specification.
Description: Operation of the time interval delay circuitry is verified by introducing a delay into a frequency measurement.


Figure 4-11. Time Interval A to B Delay Test SetapEquipment:Function GeneratorHP 3325A
Procedure:

1. Set the function generator as follows:
Frequency ..... 100 Hz
Amplitude ..... 200 mV p-p
Function Square Wave
2. Set the HP 5334B as follows:
Reinitialize the HP 5334B.
FUNCTION T.I. A $\rightarrow$ B DELAY
GATE TIME DELAY ..... 9 ms
SENS ..... ON
A \& B TRIG/SENS controls ..... fully CW
COM A ..... ON
CHAN A \& B $50 \Omega$ ..... ON
CHAN B Negative SLOPE ..... ON (falling edge)
3. Connect the function generator output to the HP 5334B Input A.
4. Press SINGLE CYCLE on the HP 5334B.

VERIFY: The Counter displays $15 \mathrm{~ms} \pm 100 \mu \mathrm{~s}$
5. Record the Time Interval Delay measurement on the Performance Test Record, line 36.

Failure: If the instrument under test does not meet the test specification, consider performing the adjustments in Section V of this manual as a first step in correcting the problem.

## 4-38. RATIO A/B TEST

Specification: Refer to Table 1-1, HP Model 5334B Specifications, for Ratio A/B specification.
Description: Two different frequencies are applied to the A and B inputs. The ratio of the A and B inputs will be displayed.


Figure 4-12. Ratio A/B Test Setup
Equipment:Function GeneratorHP 3325A
Procedure:1. Set the function generator as follows:
Frequency. ..... 5 MHz
Amplitude ..... 100 mV rms
Function ..... Sine Wave
2. Set the HP 5334B as follows:
Reinitialize the HP 5334B. FUNCTION ..... RATIO A/B
SENS ..... ON
A \& B TRIG/SENS controls. ..... fully CW
CHAN A \& B $50 \Omega$ ..... ON
3. Connect HP 5334B TIME BASE signal to Input $A$ and connect the function generator signal to Input $B$.

VERIFY: The Counter displays $2.000000 \pm 000001$.
4. Record the Ratio A/B measurement on the Test Record Card, line 37.

Failure: If the instrument under test does not meet the test specification, consider performing the adjustments in Section V of this manual as a first step in correcting the problem.

## 4-39. RISE/FALL TIME A TEST

Specification: Refer to Table 1-1, HP Model 5334B Specifications, for the Rise/Fall specifications.
Description: The Rise/Fall time function of the HP 5334B is exercised at several different frequencies and slope settings.


Figure 4-13. Rise/Fall Time A Test Setup

## Equipment:

Function Generator
HP 3325A

## Procedure:

1. Set the function generator as follows:
Frequency
10 MHz
Amplitude
.500 mV p-p
Function
Sine Wave
2. Set the HP 5334B as follows:
```
Reinitialize the 5334B.
FUNCTION
RISE/FALL A
CHANNEL A \(50 \Omega\) ON
```

3. Connect the function generator signal to the HP 5334B Input A.

VERIFY: The Counter displays $30 \mathrm{~ns} \pm 10 \mathrm{~ns}$ (Rise Time).
4. Record the rise measurement on the Performance Test Record Card, line 38.
5. Set the HP 5334B as follows:

CHAN A Negative SLOPE
VERIFY: The Counter displays $30 \mathrm{~ns} \pm 10 \mathrm{~ns}$ (Fall Time).
6. Record the fall measurement on the Performance Test Record Card, line 39.
7. Set the function generator as follows:

Frequency.
Amplitude ..................................................................................................1V p-p
Function.
Negative Ramp
VERIFY: The Counter displays $8 \mathrm{~ms} \pm 0.6 \mathrm{~ms}$ (Fall Time).
8. Record the fall measurement on the Performance Test Record Card, line 40.
9. Set the function generator as follows:

Function ..................................................................................................Positive Ramp
10. Set the HP 5334B as follows:

CHAN A Negative SLOPE OFF (rising edge)

VERIFY: The Counter displays $8 \mathrm{~ms} \pm 0.6 \mathrm{~ms}$ (Rise Time).
11. Record the rise measurement on the Performance Test Record Card, line 41.

Failure: If the instrument under test does not meet the test specification, consider performing the adjustments in Section V of this manual as a first step in correcting the problem.

## 4-40. CHANNEL C FREQUENCY RESPONSE AND SENSITIVITY TEST

This test is for HP 5334B's containing Option 030.
Specification: Refer to Table 1-1, HP Model 5334B Specifications, for the Channel C specifications.
Description: Channel C is tested at various frequencies and signal levels.


Figure 4-14. HP 5334B Channel C Frequency and
Sensitivity Setup

## Equipment:

| Signal Generato | HP 8660A/C |
| :---: | :---: |
| 10 dB Attenuator | HP 8491A |
| Adapter $\mathrm{N}(\mathrm{m})$ to $\mathrm{BNC}(\mathrm{m})$ | HP 1250-0082 |
| Adapter N(f) to BNC(f) | HP 1250-1474 |
| Adapter $\mathrm{N}(\mathrm{m})$ to $\mathrm{BNC}(\mathrm{f})$ | .HP 1250-0780 |

Procedure:

1. Set the signal generator as follows:

| Frequency. | 90 MHz |
| :---: | :---: |
| Amplitude | $-13.5 \mathrm{dBm}$ |

## NOTE

This amplitude provides 15 mV rms to the Channel C Input when using the 10 dB attenuator.
2. Set the HP 5334B as follows:
Reinitialize the 5334B.
FUNCTION
FREQ C
CHANNEL C SENSITIVITY control fully CW
3. Connect the signal generator output to the HP 5334B Input $C$ through a 10 dB attenuator.

## NOTE

The 10 dB attenuator is used here for impedance matching.

VERIFY: The Counter displays $90.0 \mathrm{MHz} \pm 2 \mathrm{~Hz}$.
4. Record the measurement on the Performance Test Record Card, line 53.
5. Set the signal generator as follows:
$\qquad$
Amplitude $-13.5 \mathrm{dBm}$

## NOTE

This amplitude provides 15 mV rms to the Channel C Input when using the 10 dB attenuator.

VERIFY: The Counter displays $200.0 \mathrm{MHz} \pm 3 \mathrm{~Hz}$.
6. Record the measurement on the Performance Test Record Card, line 54.
7. Set the signal generator as follows:

Frequency...................................................................................................... 1000 MHz
Amplitude ................................................................................................ +0.5 dBm

## NOTE

This amplitude will provide 75 mV rms to the Channel C Input when using the 10 dB attenuator.

VERIFY: The Counter displays $1000 \mathrm{MHz} \pm 20 \mathrm{~Hz}$.
8. Record the measurement on the Performance Test Record Card, line 55.
9. Set the signal generator as follows:

Amplitude
$+0.5 \mathrm{dBm}$

## NOTE

This amplitude provides 75 mV rms to the Channel C Input when using the 10 dB attenuator.

VERIFY: The Counter displays $1300 \mathrm{MHz} \pm 20 \mathrm{~Hz}$.
10. Record the measurement on the Performance Test Record Card, line 56.

Failure: Perform Section V, Adjustments, paragraphs 5-21 and 5-22.

Table 4-2. HP 5334B Performance Test Record Card

## PERFORMANCE TEST RECORD (Page 1 of 3)

| PERFORMANCE TEST RECORD (Page 1 of 3) |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| HEWLETT-PACKARD MODEL 5334B UNIVERSAL COUNTER <br> Serial Number: $\qquad$ <br> Test Performed By: $\qquad$ <br> Date: $\qquad$ <br> Notes: $\qquad$ |  | Repair/Work Order No. <br> Temperature: $\qquad$ <br> Relative Humidity: $\qquad$ <br> Post Calibration Test: $\square$ <br> Pre Calibration Test: $\square$ |  |  |  |
| $\begin{gathered} \hline \text { PARA. } \\ \text { NO. } \end{gathered}$ | TEST DESCRIPTION | $\begin{aligned} & \text { LINE } \\ & \text { NO. } \end{aligned}$ | RESULTS |  |  |
|  |  |  | MINIMUM | ACTUAL | MAXIMUM |
| 4-28. | CHANNEL A FREQUENCY RESPONSE AND SENSITIVITY TEST, $10 \mathrm{~Hz}-20 \mathrm{MHz}$ <br> Input conditions: <br> 15 mV rms <br> 10 Hz <br> DC coupled <br> 1 Megohm <br> 20 MHz <br> 15 mV rms <br> 30 Hz <br> AC coupled <br> 1 Megohm <br> 20 MHz <br> 15 mV rms <br> 1 MHz <br> AC coupled <br> 50 Ohm <br> 20 MHz | 2. 3. 4. 5. 6. | 9.07 19.9999997 29.97 19.9999997 999999.96 19.9999997 |  | 10.03 20.0000003 30.03 20.0000003 1000000.04 20.0000003 |
| 4-29. | CHANNEL B FREQUENCY RESPONSE AND SENSITIVITY TEST, $10 \mathrm{~Hz}-20 \mathrm{MHz}$ <br> Input conditions: <br> 15 mV rms <br> 10 Hz <br> DC coupled <br> 1 Megohm <br> 20 MHz <br> 15 mV rms <br> 30 Hz <br> AC coupled <br> 1 Megohm $\quad 20 \mathrm{MHz}$ <br> 15 mV rms <br> 1 MHz <br> AC coupled <br> 50 Ohm <br> 20 MHz | 7. 8. 9. 10. 11. 12. | $\begin{gathered} .07 \\ 19.97 \\ 29.97 \\ 19.97 \\ 999999.96 \\ 19.97 \end{gathered}$ |  | $\begin{gathered} 10.03 \\ 20.03 \\ 30.03 \\ 20.03 \\ 1000000.04 \\ 20.03 \end{gathered}$ |
| 4-30. | CHANNEL A FREQUENCY RESPONSE AND SENSITIVITY TEST, $80 \mathrm{MHz-100} \mathrm{MHz}$ (For Non-Option 060 Instruments, I.e., Front Inputs only) | 13. <br> 14. <br> 15. <br> 16. <br> 17. <br> 18. | 79999998.00 99999998.00 79999998.00 99999998.00 79999998.00 99999998.00 |  | 80000002.00 <br> 100000002.00 <br> 80000002.00 <br> 100000002.00 <br> 80000002.00 <br> 100000002.00 |

Table 4-2. HP 5334B Performance Test Record Card (Continued)
PERFORMANCE TEST RECORD (Page 2 of 3)

| PERFORMANCE TEST RECORD (Page 2 of 3) |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| PARA NO. | TEST DESCRIPTION | $\begin{array}{\|l\|} \hline \text { LINE } \\ \text { NO. } \end{array}$ | RESULTS |  |  |
|  |  |  | MINIMUM | ACTUAL | MAXIMUM |
| 4-31. | CHANNEL B FREQUENCY RESPONSE AND SENSITIVITY TEST, $10 \mathrm{~Hz}-20 \mathrm{MHz}$ (For Non-Option 060 Instruments, i.e., Front Inputs only) |  |  |  |  |
|  | Input conditions: |  |  |  |  |
|  | 35 mV rms DC coupled | 19. | 79999998.00 |  | 80000002.00 |
|  | 1 Megohm $\quad 100 \mathrm{MHz}$ | 20. | 99999998.00 |  | 100000002.00 |
|  | 35 mV rms AC coupled $\quad 80 \mathrm{MHz}$ | 21. | 79999998.00 |  | 80000002.00 |
|  | 1 Megohm $\quad 100 \mathrm{MHz}$ | 22. | 99999998.00 |  | 100000002.00 |
|  | 35 mV rms AC coupled $\quad 80 \mathrm{MHz}$ | 23. | 79999998.00 |  | 80000002.00 |
|  | $50 \mathrm{Ohm} \quad 100 \mathrm{MHz}$ | 24. | 99999998.00 |  | 100000002.00 |
| 4-32. | CHANNEL A FREQUENCY RESPONSE AND SENSITIVITY TEST, $10 \mathrm{~Hz}-20 \mathrm{MHz}$ (For Option 060 Instruents, i.e., Front and Rear Inputs) |  |  |  |  |
|  | Input conditions: |  |  |  |  |
|  | 50 mV rms DC coupled $\quad 80 \mathrm{MHz}$ | 25. | 79999998.00 |  | 80000002.00 |
|  | 1 Meghohm 100 MHz | 26. | 99999998.00 |  | 100000002.00 |
|  | 50 mV rms AC coupled $\quad 80 \mathrm{MHz}$ | 27. | 79999998.00 |  | 80000002.00 |
|  | 1 Megohm $\quad 100 \mathrm{MHz}$ | 28. | 99999998.00 |  | 10000002.00 |
| 4-33. | CHANNEL B FREQUENCY RESPONSE AND SENSITIVITY TEST, $80 \mathrm{MHz}-100 \mathrm{MHz}$ (For Option 060 Instruments, i.e., Front and Rear Inputs) <br> Input conditions: |  |  |  |  |
|  | $\begin{aligned} & 50 \mathrm{mV} \text { rms } \\ & \text { DC coupled } \end{aligned} \quad 80 \mathrm{MHz}$ | 29. | 79999998.00 |  | 80000002.00 |
|  | 1 Megohm $\quad 100 \mathrm{MHz}$ | 30. | 99999998.00 |  | 100000002.00 |
|  | $\begin{aligned} & 50 \mathrm{mV} \text { rms } \\ & \text { AC coupled } \end{aligned} \quad 80 \mathrm{MHz}$ | 31. | 79999998.00 |  | 80000002.00 |
|  | $1 \mathrm{Megohm} \quad 100 \mathrm{MHz}$ | 32. | 99999998.00 |  | 100000002.00 |
| 4-34. | PERIOD A TEST <br> 50 mV rms, 100 MHz , sine wave | 33. | 9.9999999 ns |  | 10.0000001 ns |
| 4-35. | PULSE WIDTH A TEST <br> 200 mV rms, 100 MHz , sine wave | 34. | 1 ns |  | 9 ns |
| 4-36. | TIME INTERVAL A TO B TEST 200 mV p-p, 5 MHz , square wave | 35. | 94 ns |  | 106 ns |
| 4-37. | TIME INTERVAL A TO B DELAY TEST 200 mV p-p, 100 Hz , square wave | 36. | 14.9 ms |  | 15.1 ms |
| 4-38. | RATIO A/B 100 mV rms, 5 MHz , sine wave | 37. | 1.999999 |  | 2.000001 |

Table 42. HP 5334B Performance Test Record Card (Continued)

| PERFORMANCE TEST RECORD (Page 3 of 3) |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{array}{c\|} \hline \text { PARA. } \\ \text { NO. } \end{array}$ | TEST DESCRIPTION | $\begin{aligned} & \text { LINE } \\ & \text { NO. } \end{aligned}$ | RESULTS |  |  |
|  |  |  | MINIMUM | ACTUAL | MAXIMUM |
| 4-39. | RISE/FALL TIME A TEST |  |  |  |  |
| 4-40. | 500 mV p-p, 100 MHz , sine wave (rise) (fall) <br> (fall) <br> (fall) | $\begin{aligned} & 38 . \\ & 39 . \\ & 40 . \\ & 41 . \end{aligned}$ | $\begin{gathered} 20 \mathrm{~ns} \\ 20 \mathrm{~ns} \\ 7.4 \mathrm{~ms} \\ 7.4 \mathrm{~ms} \end{gathered}$ |  | 40 ns 40 ns 8.6 ms 8.6 ms |
|  | CHANNEL C FREQUENCY RESPONSE AND SENSITIVITY TEST |  |  |  |  |
|  | $\begin{aligned} & \text { - } 13.5 \mathrm{dBm}, 90 \mathrm{MHz} \\ & \text {-13.5 dBm, } 200 \mathrm{MHz} \\ & \text { + } 0.5 \mathrm{dBm}, 1000 \mathrm{MHz} \\ & \text { + } 0.5 \mathrm{dBm}, 1300 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 38 . \\ & 39 . \\ & 40 . \\ & 41 . \end{aligned}$ | $\begin{gathered} 89999998 \\ 199999997 \\ 999999980 \\ 129999998 \end{gathered}$ |  | $\begin{gathered} 90000002 \\ 200000003 \\ 1000000020 \\ 1300000020 \end{gathered}$ |

## 4-41. HP-IB VERIFICATION TEST

4-42. The following test checks the Counter's ability to process or send the HP-IB Messages (Meta Messages) described in Table 3-9. During the test all of the Counter's HP-IB data input/output bus, control, and handshake lines are checked. Only the Counter, an HP 85A, or 85B controller, an HP-IB interface with appropriate cabling, and an HP-IB Verification Cassette, HP P/N 59300-10002, Revision K (or later) are needed for the test setup. If desired, an HP 9000 Series $200 / 300$ controller may be used with an HP-IB Verification program written in HP Basic 5.xx. The disc part numbers are 05334-13501 (3.50") and 05334-13502 (5.25").

4-43. The validity of these checks is based on the following assumptions:

- The Counter operates correctly from the front panel. This can be verified by performing the Operational Verification Tests beginning with paragraph 4-12.
- The controller properly executes HP-IB operations.
- The HP-IB interface properly transfers the controller's instructions.

4-44. If the Counter appears to fail any of the HP-IB checks, the validity of the above assumptions should be confirmed before servicing the Counter.

4-45. The select code of the controller's I/O is assumed to be 7. The address of the controller is assumed to be 21. This select code-address combination, (i.e., 721) is necessary for these checks to be valid. The program lines presented here would have to be modified for any other combination.

4-46. If all of these checks are performed successfully, the Counter's HP-IB capability can be considered to be performing properly. These procedures do not check whether or not all of the Counter's program commands are being properly interpreted and and executed by the instrument, however, if the front panel operation is confirmed to be working properly and its HP-IB capability operates correctly, then there is a high probability that the Counter will respond properly to all of its program commands.


Figure 4-15. HP-IB Verification Test Setup

## Equipment:

```
Controller
HP 85A or 85B
ROM Drawer HP 82936A
I/O ROM...............................................................................................................HP 00085-15003
16K Memory Module, (85A only) .....................................................................HP 82903A
HP-IB Interface Card/Cable HP 82937A
```


## Procedure:

The HP 85 program is listed in Table 4-4. It is an interactive program and almost completely self-exlanatory. The HP Basic program is not included in this manual, but is available upon request. Please contact your local HP Sales office for more information.

1. Connect the equipment as shown in Figure 4-15.
2. To run the program, insert the cassette in the HP 85 and power-up the controller. If the controller is already ON, insert the cassette and type:

## CHAIN "Autost"

then press END LINE.
3. Press the soft key corresponding to HP 5334B, and follow the instructions displayed on the HP 85 screen.
4. The program automatically starts and displays the program title, then it displays the following checkpoint summary: summary:

## CHECKPOINT SUMMARY



```
1 Power-up Preset
2 Remote, Local, Local Lockout
3 Function Select
4 Input Conditioning - Channel A
5 Input Conditioning - Channel B
6 Trigger Levels
7 Gate Time
8 External Arming
9 Math Functions
10 Memory Recall (HP 5334A only)
1 1 \text { Service Request}
12 Status Byte
1 3 \text { Send Error Code}
1 4 \text { High Speed Output}
```

5. The next screen provides the option to receive a printed version of this summary.
6. Equipment setup instructions are provided (with reference made to the manual), then the HP 85 searches for the address of the HP 5334B. This search eliminates the need to set the HP 5334B to a particular HP-IB address and thus, allows an arbitrary address setting. If the address is not found, one or more of the following may be the cause:
```
HP 5334B - not powered-up
    - in TALK ONLY mode (Addr 50)
Interface - not connected
    - defective
```

Address of
HP 5334B - set to 721 (controller address)
- set to 731-749 (not valid addresses)
7. After these initial steps, the program begins the checkpoint execution. The HP 85 display provides the description and operator instructions as each checkpoint is performed.
8. At the end of most of the checkpoints, the HP 85 displays the following prompt:

Press the softkey corresponding to the results of this checkpoint ...

PASS - Press K1 to indicate that

- the $5334 \mathrm{~A} / \mathrm{B}$ passed.

FAIL - Press K4 to indicate that the $5334 \mathrm{~A} / \mathrm{B}$ failed.

PASS
FAIL
9. As instructed, pressed the soft key corresponding to the checkpoint results.
10. For checkpoints 11,12 , and 13 , one of the following messages will be displayed instead of the above message:

The HP 85 has verified that the 5334A/B passed this checkpoint.
or
The HP 85 has verified that the 5334A/B failed this checkpoint.

As indicated, the HP 85 has been instructed to verify the results of the checkpoint and display its decision.
11. The next screen displayed by the HP 85 is shown below:

Press a soft key to select the desired checkpoint ...

NEXT - Press K1 to perform the next checkpoint.

REPEAT - Press K3 to repeat this checkpoint.

GOTO\# - Press K4 to select an arbitrary checkpoint.

| NEXT | REPEAT | GOTO\# |
| :---: | :---: | :---: |

12. The format of the program allows the user to proceed in a sequential order to the next checkpoint, repeat the present checkpoint, or go to an arbitrary checkpoint.
13. When "GO TO \#" has been selected, the following prompt occurs:
```
Enter checkpoint number desired (0 to 14), and press END LINE (0 TERMINATES PROGRAM).
?
```

14. Entering a number other than 0 causes that checkpoint to be executed. If 0 is entered, the program terminates by displaying the checkpoint results, and providing the option to receive a printed version. An example of the printed checkpoint results is shown below:

CHECKPOINT RESULTS
FOR HP-IB ADDRESS 703

| CHECKPOINT | 1 PASS |
| :--- | :--- |
| 2 | 2 PASS |
| 3 | PASS |
| 4 | FAIL |
| 5 | NOT PERFORMED |
| 6 | PASS |
| 7 PASS |  |
| 8 | NOT PERFORMED |
| 9 | 10 FASS |
| 11 | NOT PERFORMED |
| 12 NOT PERFORMED |  |
| 13 PASS |  |
| 14 FAIL |  |



```
10 ! ****** HP 5334A/B
50 ! JD
60 ! DATE : 15 MARCH 1987
70: REUISION B
80!
90
100 ! of its command code set via HP-IB. The program consists
110 ! of 14 checkpoints, and provides the user with the ability
120 ! to execute and repeat these tests in any order.
130 ! Also provided are options to print the checkpoint
140 ! summary and results. The program relies heavily on
150 ! subroutines in addition to arrays and simple variables.
160
170
180! A (Address)
190 ! B (Eyte information)
200! C (CRT status)
210! 0 (Decision)
220 ! E (Error value)
230 ! F (0PT 700 FLAG)
240 ! I (Loop variable)
250 ! J (Loop variable)
260 ! L (Trigger levels)
270 ! M (SRQ Byte information)
280 ! F (Result variable)
290 ! R() (Result array)
300 ! S (Step number)
310 ! U \Value of tyte)
320
330
340 NORMAL
350 ! DIMENSION AND INITIALIZE STRING UARIABLE ARRAYS
360 DIM A$[30],E$[30],C$[35],D$[35],E$[30],F$[30],G$[30],H$[35]
370 DIM R$[30],5$[30]
380 DIM I电[35],J$[10],K$[10],L$[21],M$[21],N$[10],R(14),X(5),X$[300]
390 A$="Press CONT to perform test."
400 B$="Press CONT when ready."
C$="Verify that 5334A/E front panel"
D$="Verify that 53J4A/B display"
E$="After pressing CONT,
F$="Fress CONT for next display.
G$=" CHECKPOINT "
H$="**********************************"
!
FOR I=1 TO 14
R(I)=\emptyset
NEXT I
CRT IS I
```

```
520 C=1
530 ENABLE KBD 1+32
540!
550 ! DISPLAY TITLE, CHECKPOINT LIST AND SETUP INSTRUCTIONS
560 BEEP
5 7 0 \text { CLEAR}
580 DISP USING "5/"
590 DISP H$
600 DISP
610 DISP " 5334A/B HP-IB OPERATION"
620 DISP " UERIFICATION PROGRAM"
630 DISP
6 4 0 ~ D I S P ~ H \$ ~
6 5 0 ~ D I S P
660 WAIT 2500
6 7 0 \text { CLEAR}
680 DISP USING "5/"
690 DISP H$
7 0 0 \text { DISP}
710 DISP " CHECKPOINT SUMMARY"
7 2 0 \text { DISP}
7 3 0 ~ D I S P ~ H \$ ~
740 DISF
750 IF C=2 THEN 780
760 WAIT 2000
7 7 0 \text { CLEAR}
780 DISP " 1 Power-up Preset"
790 DISP " 2 Remote, Local, Local Lockout"
800 DISP " 3 Function Select"
810 DISP " 4 Input Conditioning-Channel A"
820 DISP " 5 Input Conditioning-Channel B"
830 DISP " 6 Trigger Levels"
840 DISP " 7 Gate Time"
850 DISP " 8 External Arming"
860 DISP " }9\mathrm{ Math Functions"
870 DISP "10 Memory Recall (5334A only)"
880 DISP "11 Service Request"
890 DISP "12 Status Byte"
900 DISP "13 Send Error Code"
910 DISP "14 High Speed Output"
920 IF C=2 THEN DISP USING "5/," @ GOTO 1090
930 DISP USING "#,K,/," ; F$
940 PAUSE
950 CLEAR
960 DISP "Would you like a printed versionof the checkpoint summary?"
970 DISP
980 DISP "YES - Fress K1 to receive a printed version."
990 DISP
1000 DISP "NO - Press K4 to proceed."
1010 ON KEY# 1,"YES" GOTO 1050
1020 ON KEY# 4," NO" GOTO 1110
```

```
1030 KEY LABEL
1040 GOTO 1040
1050 CLEAR
1060 CRT IS 2
1070 C=2
1080GOTO 690
1090 CRT IS I
1100C=1
1110 CLEAR
1120 DISP "The HP }85\mathrm{ should have an I/O ROMin its ROM Drawer, a 16K Memory"
1130 DISP "Module, and an 82937A HP-IB Interface Card/Cable."
1140 DISP
1150 DISP "Connect the HP-IB Interface to the rear panel of the HP 5334A/B"
1160 DISP "and power-up the instrument."
1170 DISP
1180 DISP "Consult the HP 5334A/B Operatingand Programming Manual for"
1190 DISP "additional information."
1200 DISP
1210 DISP B$
1220 PAUSE
1230 CLEAR
1240!
1250 ! TEST FOR OPTION 700
1260 DISP
1270 DISP "Does instrument have OPTION 700 installed?"
1280 DISP
1290 DISP "YES - Press Kil"
1300 DISP
1310 DISP "NO - Press K4"
1320 ON KEY# 1," YES" GOTO 1370
1330 ON KEY# 4," NO" GOTO 1380
1340 KEY LABEL
1350 GOTO 1350
1360 CLEAR
1370 F=1 @ GOTO 1390
1380 F=2
1390 ! INPUT 5334A/B ADDRESS
1400 CLEAR
1410 N$="NOT5334A/B"
1420 DISP "Input 5334A/B address"
1430 DISP
1440 DISP "Example: 703"
1450 DISP
1460 DISP "Press END LINE after entry"
1470 INPUT A
1480 CLEAR
1490 SET TIMEOUT 7;300
1500 IF F=2 THEN 1530
1510 OUTPUT A ; "GAL."
1520 WAIT 1000
1530 REMOTE A
1540 OUTPUT A ;"ID"
```

```
1550 ENTER A ; N$
1560 IF N$="HP5334A" THEN 1770
1570 IF N$="HP5334B" THEN 1770
1580 CLEAR A
1590 ABORTIO 7
1600 BEEP
1610 WAIT 250
1620 BEEP
1630 DISP "No response at that address"
1640 DISP
1650 DISP "Verify HP-IB connection, option configuration, the 5334A/B is on"
1660 DISP "and not in the TALK ONLY mode."
1670 DISP
1680 DISP "An ERROR message on the 5334A/B denotes an INCORRECT answer"
1690 DISP "to OPTION 700 question..."
1700 DISP
1710 DISP "If an ERROR occurred:"
1720 DISP "* Recheck option configuration"
1730 DISP "* Cycle power switch on 5334A/B"
1740 DISP "* Press RUN to restart program"
1750 PAUSE
1760 GOTO 1400
1770 DISP
1780 DISP "HP 5334A/B found at address";A
1790 WAIT 3000
1800 CLEAR
1810 DISP
1820 DISP " *** NOTE *** "
1830 DISP
1840 DISP "An ERROR message on the 5334A/B denotes an INCORRECT answer "
1850 DISP "to OPTION 700 question...
1860 DISP
1870 DISP "If an ERROR occurred:"
1880 DISP " * Recheck option configuration"
1890 DISP " * Cycle power switch on 5334A/B"
1900 DISP " * Press RUN to restart program"
1910 DISP
1920 DISP "Otherwise, press CONT"
1930 DISP
1940 PAUSE
1950 SET TIMEOUT 7;0
1960 !
1970 ! CHECKPOINT I
1980 I $=" Power-up Preset"
1990 S=1
2000 GOSUB 7810
2010 DISP "Toggle the 5334A/B line switch from ON to OFF, then back to ON."
2020 DISP
2030 DISP "Verify that all lamps turn on"
2040 DISP "momentarily, the display flashes"
2050 DISP "'HP 5334A' or 'HP 5334b', the"
```

```
2050 DISP "HP-IB address, and the word"
2070 DISF ",PASS'"
2080 DISP B$
2090 FAUSE
2100 CLEAR
2110 DISP "The counter goes through an ex-tensive self test on power up."
2120 DISP "If any failures are found, they are immediately indicated with aFAIL
message."
2130 DISP
2140 IF F=1 THEN 2170 ! Option 700 installed.
2150 DISP "PRESET, Hz, FREQ A and AUTO TRIGannunciators are lit."
2160 GOTO 2180
2170 DISP "PRESET, Hz, FREQ A, AUTO TRIG and DISABLE annunciators are lit."
2180 DISP
2190 DISP D$;"shows --------"
2200 DISP
2210 DISP
2220 DISP USING "#,K,/," ; F$
2230 PAUSE
2240 IF F=2 THEN 2250
2250 OUTPUT A ;"GAL"
2260 GOT0 7960
2270 !
2280 ! CHECKPOINT 2
2290 I $=" Remote, Local, Local Lockout"
2300 S=2
2310 605UB 7810
2320 LOCAL 7
2330 ABORTIO }
2340 DISF E里;"the" 5334A/B"
2350 DISP "will be placed under remote control."
2360 GOSUB 8480
2370 REMOTE A
2380 CLEAR
2390 DISP "Verify that the REMOTE and LISTEN status LEDs are lit."
2400 DISP
2410 DISP F$
2420 PAUSE
2430 CLEAR
2440 DISP E$;"the 5334A/B"
2 4 5 0 ~ D I S P ~ " w i l l ~ b e ~ p l a c e d ~ i n ~ t h e ~ L O C A L ~ L O C K O U T ~ m o d e . " ~
2460 GOSUE 8450
2470 REMOTE A
2480 LOCAL LOCKOUT }
2490 CLEAR
2 5 0 0 ~ D I S P ~ " P r e s s ~ t h e ~ f r o n t ~ p a n e l ~ L O C A L ~ k e y ~ t o ~ v e r i f y ~ t h a t ~ t h e ~ 5 3 3 4 A / B ~ i s ~ i n " ~
2510 DISP "LOCAL LOCKOUT and remains in REMOTE.
2520 0ISP
2530 DISP F$
2540 PAUSE
2550 CLEAR
```

```
2560 DISP E&;"the 5334A/B"
2570 DISP "will be placed in the LOCAL mode."
2580 GOSUB 8480
2590 LOCAL 7
2600 CLEAR
2610 DISP C$
2620 DISP "REMOTE status LED is now unlit."
2630 GOTO 7910
2640!
2650 ! CHECKPOINT 3
2660 I$=" Function Select"
2670 5=3
2680 GOSUB 7810
2650 DISP E$; "verify that"
2700 DISP "the FUNCTION key button annunciators light in sequence"
2710 DISP "from FREQ A to DUM and back to FREQ A. A tone will sound"
2720 DISP "to mark each function change."
2730 DISP
2740 DISP USING "#,K,/" ; A生
2750 PAUSE
2760 REMOTE A
2770 OUTPUT A ;"IN"
2780 WAIT 1000
2790 OUTPUT A ;"FNI"
2800 GOSUB 8540
2810 OUTPUT A ;"FN2"
2820 GOSUB 8540
2830 OUTPUT A ; "FN3"
2840 GOSUB 8540
2850 OUTPUT A ; "FN4"
2860 GOSUB 8540
2870 OUTPUT A ; "FN5"
2880 G0SUB 8540
2890 OUTPUT A ; "FNG"
2900 GOSUB 8540
2910 OUTPUT A ; "FN7"
2920 GOSUB 8540
2930 OUTPUT A ;"FN8"
2940 GOSUE 8540
2950 OUTPUT A ; "FNS"
2960 GOSUB 8540
2970 OUTPUT A ; "FN10"
2980 GOSUB 8540
2990 OUTPUT A ;"FN11"
3000 G0SUB 8540
3010 OUTPUT A ; "FN12"
3020 GOSUB 8540
3030 OUTPUT A ; "FN1"
3040 GOTO 7960
3050 !
3060 : CHECKPOINT 4
```

```
3070 I$=" Input Conditioning-Channel A"
3080 S=4
3090 GOSUB 7810
3100 DISP E$;"verify that"
3110 DISP "the display annunciators SLOPE,"
3120 DISP "X10, AC, 50 Z, FILTER A, and COMA light (in that order) for"
3130 DISP "INPUT A. A tone will sound to"
3140 DISP "mark each input change."
3 1 5 0 ~ D I S P
3160 DISP A$
3170 PAUSE
3180 REMOTE A
3190 OUTPUT A ;"IN AUD"
3200 WAIT 1000
3210 OUTPUT A ;"AS1"
3220 GOSUB 8540
3230 OUTPUT A ;"AS0 AX1"
3240 GOSUB 8540
3250 OUTPUT A ; "AX0 AA1"
3260 GOSUB 8540
3270 OUTPUT A ; "AAD AZ1"
3280 GOSUB 8540
3290 OUTPUT A ; "AZ0 FI1"
3300 GOSUB 8540
3310 OUTPUT A ;"FI0 COI"
3320 GOSUB 8540
3330 OUTPUT A ;"CO0
3340 CLEAR
3350 DISP "The 5334A/B is in the READ PEAKS Amode."
3360 DISP
3370 OUTPUT A ;"IN FN14 "
3380 DISP D$;"shows '0.00 0.00 A'."
3390 DISP
3400 DISP F$
3410 PAUSE
3420 CLEAR
3430 OUTPUT A ;"IN AU0"
3440 GOTO 7960
3450!
3460 : CHECKPOINT 5
3470 I$=" Input Conditioning-Channel B"
3480 S=5
3490 GOSUB 7810
3500 DISP E$;"verify that"
3510 DISP "the display annunciators SLOPE,"
3520 DISP. "X10, AC, and 50 Z light (in thatorder) for INPUT B. A tone will"
3530 DISP "sound to mark each input change."
3540 DISP
3550 DISP USING "#,K,/" ; A虫
3560 PAUSE
3570 REMOTE A
3580 OUTPUT A ;"IN AUO
```


## Table 4-4. HP-IB Operational Verification

Program Listing (Continued)

```
3 5 9 0 ~ W A I T ~ 1 0 0 0 ~
3600 OUTPUT A ;"BSI"
3610 GOSUB 8540
3620 OUTPUT A ;"BS0 BXI"
3630 G0SUB 8540
3640 OUTPUT A ; "BX0 BA1"
3650 GOSUB 8540
3660 OUTPUT A ;"BAD BZ1"
3670 GOSUB 8540
3680 OUTPUT A ;"BZD IN AU0 "
3690 CLEAR
3700 DISP "The 5334A/B is in the READ PEAKS Bmode."
3 7 1 0 ~ D I S P
3 7 2 0 ~ O U T P U T ~ A ~ ; " I N ~ F N I S ~ " '
3730 DISP D$;"shows '0.00 0.00 b'."
3740 DISP
3750 DISP F$
3760 PAUSE
3770 CLEAR
3780 OUTPUT A ;"IN AUO"
3790 GOTO 7960
3800 !
3810 ! CHECKPOINT 6
3820 I$=" Trigger Levels
3830 S=6
3840 G0SUB 7810
3850 DISP E$;"the 5334A/B"
3860 DISP "will be programmed to the trigger levels below."
3870 DISP
3880 DISP "-2.34 1.56 L"
3890 DISP
3900 PAUSE
3910 REMOTE A
3920 OUTPUT A ;"TR0 SE0"
3930 OUTPUT A ;"AT-2.34 BT+1.56"
3540 OUTPUT A ;"TR1 FN13"
3950 CLEAR
3960 DISP D$
3970 DISP "reads '-2.34 1.5E L'."
3980 DISP
3990 DISP F$
4000 PAUSE
4010 CLEAR
4020 DISP "Press RESET/LOCAL."
4030 DISP "Press READ LEVELS 4 times."
4040 DISP
4 0 5 0 ~ D I S P ~ " T h i s ~ s e q u e n c e ~ a l l o w s ~ t h e ~ t r i g g e r l e v e l ~ c o n t r o l ~ t o ~ r e t u r n ~ t o ~ t h e ~ f r o n t
panel."
4060 DISF
4 0 7 0 \text { DISP "Adjust the A and B LEVEL knobs for a different level reading."}
4080 DISP E&;"check that"
```

```
4090 DISP "the correct levels are read."
4 1 0 0 ~ P A U S E
4110 WAIT 1000
4120 CLEAR
4130 OUTPUT A ;"FN13"
4140 ENTER A ; L$
4 1 5 0 ~ D I S P ~ " T r i g g e r ~ l e v e l s ~ r e a d ~ a r e , " ~
4160 DISP L$
4170 DISP
4180 DISP F$
4190 PAUSE
4200 WAIT 1000
4210 OUTPUT A ;"IN"
4220 GOTO 7960
4230
```



```
4250 I $=" GATE TIME"
4260 S=7
4270 GOSUB 7810
4280 DISP E$;"verify that"
4290 DISP "the SINGLE CYCLE and 100-GATE"
4300 DISP "AVERAGE display annunciators light. A tone will sound"
4310 DISP "to mark the function change."
4320 PAUSE
4 3 3 0 ~ R E M O T E ~ A ~
4340 OUTPUT A ;"GS1"
4 3 5 0 ~ G O S U B ~ 8 5 4 0 ~
4360 OUTPUT A ;"GSD GU1"
4370 GOSUB 8540
4 3 8 0 ~ C L E A R ~
4390 DISP "Verify that the GATE TIME is setto 1.230 seconds by pressing GATE
TIME."
4400 OUTPUT A ;"GU0 GA1.23"
4410 LOCAL A
4420 GOTO 7910
4430 !
4440 ! CHECKPOINT 8
4450 I $=" External Arming
4460 S=8
4470 GOSUB 7810
4480 R=1
4 4 9 0 ~ D I S P ~
4500 DISP "Press EXT ARM SELECT on the 5334A/B. Verify that the front "
4510 DISP "panel reads 'St - SP -'."
4 5 2 0 ~ D I S P
4530 REMOTE A
4540 OUTPUT A ;"XAZ XO2"
4550 LOCAL A
4560 DISF F$
4 5 7 0 ~ P A U S E
4580 CLEAR
4590 REMOTE A
```

```
4600 DISP "The 5334A/B will now be pro- grammed for POSITIVE external"
4610 DISP "start and stop arm."
4620 DISF
4630 DISP "Press EXT ARM SELECT to verify this."
4640 REMOTE A
4650 OUTPUT A ; "XA1 X01"
4660 LOCAL A
4E70 OISP
4680 DISP B$
4 6 9 0 ~ P A U S E ~
4700 CLEAR
4710 DISP "Lastly, the 5334A will be pro- grammed for NEGATIUE external"
4720 DISP "start and stop arm slopes."
4 7 3 0 ~ D I S P
4740 DISP "Press EXT ARM SELECT to verify this."
4 7 5 0 ~ R E M O T E ~ A ~
4760 OUTPUT A ;"XA3 X0J"
4770 LOCAL A
4780 DISP
4790 DISP B$
4800 PAUSE
4810 CLEAR
4820 G0SUB 7960
4830 !
4840 ! CHECKPOINT g
4850 I $=" Math Function Test"
4860 S=9
4870 GOSUB 7810
4880 R=1
4890 DISP ES;"math offset"
4 9 0 0 ~ D I S F ~ " a n d ~ n o r m a l i z e ~ c o n s t a n t s ~ w i l l ~ b e " ~
4910 DISP "entered in the 5334A/B. The OFS"
4920 DISP "and NML indicators on the"
4930 DISP "53J4A/B front panel will light."
4940 GOSUB 8490
4 9 5 0 ~ R E M O T E ~ A ~
4960 OUTPUT A ;"IN "
4970 OUTPUT A ;"MDO MNZ.55 MO2.0"
4 9 8 0 ~ W A I T ~ 1 0 0 0 ~
4990 LOCAL A
5000 CLEAR
5010 DISP "Verify OFS and NML indicators are lit."
5 0 2 0 ~ D I S P
5030 DISF "To check that the constants are"
5040 DISP "entered, press the SELECT/ENTER"
5050 DISF "key, and verify that the 5334A/B"
5050 DISP "front panel reads '2.0'."
5 0 7 0 ~ D I S P ~
5080 DISP "Press the SELECT/ENTER key"
5090 DISP "again. The display should read"
5100 DISP "'3.55'."
5110 DISP
```

```
5120 DISP F$
5130 PAUSE
5140 REMOTE A
5150 OUTPUT A ;"IN"
5160 G0SUB 7960
5170 !
5180: CHECKPOINT 10
5190 I\Phi=" Memory Recall "
5200 5=10
5210 GOSUB 7810
5220 DISP N$
5230 DISP
5240 IF N$="HP5334A" THEN 5320
5250 DISP "The 5334B does not have"
5260 DISP "this function."
5270 DISP
5280 DISF B$
5290 PAUSE
5300 GOSUB 8170
5 3 1 0 \text { GOTO 8420}
5 3 2 0 ~ R E M O T E ~ A ~
5330 OUTPUT A ;"IN"
5340 DISP E$;"the 5334A"
5350 DISP "will be programmed to a certain measurement setup which will then
be stored."
5360 PAUSE
5 3 7 0 \text { CLEAR}
5380 DISP "Verify that the TI A-B and SINGLE CYCLE annunciators are lit."
5390 DISP
5 4 0 0 ~ D I S P ~ " P r e s s i n g ~ C O N T ~ a g a i n ~ w i l l ~ c a u s e ~ t h e ~ c o u n t e r ~ t o ~ d o ~ a ~ p o w e r - u p ~ r e s e t
."
5410 OUTPUT A ;" FN5 TRI AT1.5 BT1.2 GS1 GA.4 "
5420 PAUSE
5430 OUTPUT A ;"MSS"
5440 OUTPUT A ;"CK "
5450 BEEP
5460 CLEAR
5470 DISP ES;"the counter"
5480 DISF "will recall its previous state."
5 4 9 0 ~ P A U S E ~
5500 CLEAR
5510 DUTPUT A ;"MRG"
5520 LOCAL A
5530 DISP "Verify that the counter is in the TIME INTERUAL mode."
5540 DISP "The SINGLE CYCLE annunciator is lit. Press READ LEVELS"
5550 DISP "and verify that the display reads '1.50 1.20 L'."
5560.0ISP
5570 DISP F$
5580 PAUSE
5590 GOTO 7960
5600!
```

```
5610 : CHECKPOINT 11
5620 I$=" Service Request"
5630 S=11
5640 G0SUB 7810
5650 DISP "For this test, connect the TIME"
5660 DISP "BASE Output from the back panel"
5670 DISP "of the 5334A/B to INPUT CHANNEL A using a BNC cable"
5 6 8 0 ~ D I S P
5690 DISP B$
5 7 0 0 ~ P A U S E
5710 CLEAR
5720 DISP E$;"the counter"
5 7 3 0 ~ D I S P ~ " w i l l ~ c o u n t ~ t h e ~ t i m e ~ b a s e , ~ a n d ~ s e r v i c e ~ r e q u e s t ~ m a s k ~ w i l l ~ b e " ~
5 7 4 0 \text { DISP "set. The SRQ lamp will flash"}
5 7 5 0 ~ D I S P ~ " 5 ~ t i m e s ~ o n ~ t h e ~ c o u n t e r , ~ a n d ~ t h e " ~
5760 DISP "HP 85 screen will display the "
5770 DISP "count 5 times."
5780 DISP
5790 DISP USING "#,K,/" ; A$
5800 PAUSE
5810 REMOTE A
5820 OUTPUT A ; "IN FNI GAI SMI3 WAI"
530 CLEAR
5840 I=0
580 STATUS 7,1 ; Z
5860 ON INTR 7 GOTO 5900
5870 ENABLE INTR 7;8
5880 IF I =0 THEN DISP "Is BNC cable connected?"
5890 G0T0 5890
5900 M=SPOLL(A)
5910 IF BIT(M,2) THEN GOTO 6070
5 9 2 0 ~ I F ~ B I T ( M , 3 ) ~ T H E N ~ G O T O ~ 6 0 7 0 ~
5930 ENTER A ; M$
5940 IF I=0 THEN CLEAR
5 9 5 0 ~ D I S P ~ M \$ ~
5 9 6 0 ~ I = I + 1
5970 IF I<S THEN GOTO 5870
5980 CLEAR
5 9 9 0 ~ D I S P
G000 DISP "Disconnect BNC cable."
6 0 1 0 ~ D I S P ~
6020 DISP F$
6 0 3 0 ~ P A U S E ~
6040 G0T0 7960
6050 STATUS 7,1 ; Z
60G0 CLEAR
6070 R=0
6080 G0SUB 8750
6090 DISP "Disconnect BNC cable."
6 1 0 0 ~ D I S P
6110 DISP F$
6 1 2 0 ~ P A U S E ~
```

```
6130 G0T0 7970
6140!
6150 ! CHECKPOINT }1
6160 I$=" Status Byte"
6170 5=12
6180 GOSUB 7810
6190 R=1
6200 DISP E$;"the 5334A/B"
6 2 1 0 ~ D I S P ~ " w i l l ~ b e ~ r e s e t , ~ a n d ~ t h e ~ s t a t u s ~ b y t e ~ w i l l ~ b e ~ r e a d ~ b y ~ t h e " ~
6220 DISP "controller."
6230 GOSUB 8480
6240 REMOTE A
6250 OUTPUT A ;"CK"
6260 GOSUB 8600
6270 GOSUB 8750
6280 GOTO 7970
6290 !
6300 ! CHECKPOINT 13
6310 I$=" Send Error Code"
6320 5=13
6330 GOSUB 7810
6340 R=1
6350 DISP E$;"an"
6360 DISP "unrecognizable command code willbe sent to the 5334A/E to
                                    gener
ate an error."
6370 GOSUB 8480
6380 REMOTE A
6390 OUTPUT A ; "INVALID COMMAND"
6400 CLEAR
6410 DISP "Verify that the 5334A/B display shows 'ERROR 4.0'."
6 4 2 0 ~ D I S P ~
6430 DISP E$;"the error"
6440 DISP "for this illegal command will besent to the controller."
6450 GOSUB 8480
6460 LOCAL 7
6470 WAIT 3000
6480 E=0
6 4 9 0 ~ C L E A R ~
6500 DISP "The expected value for this error code is 4 ."
6 5 1 0 ~ R E M O T E ~ A ~
6520 OUTPUT A ;"TE"
6530 ENTER A ; E
6540 [ISP
6550 DISP "The returned value for this error code is ";E;"."
6560 IF E=4 THEN R=R*1
6570 IF E<>4 THEN R=R*D
6580 DISP
6590 DISP F$
6 6 0 0 ~ P A U S E ~
6610 CLEAR A
6E20 GOSUB }875
6630 !
```

```
6640 ! CHECKPOINT 14
6650 I$=" High Speed Output"
6660 S=14
6670 GOSUB 7810
6680 REMOTE A
6690 OUTPUT A ;"IN"
6700 IOBUFFER X$
6710 DISP "In this test, the 5334A/B"
6720 DISP "will be programmed to output frequency in the high speed data"
6730 DISP "output mode. For this test, connect a BNC cable from the"
6 7 4 0 \text { DISP "Time Base Output on the 53J4A/B"}
6 7 5 0 ~ D I S P ~ " b a c k ~ p a n e l ~ t o ~ I N P U T ~ A . " '
6 7 6 0 ~ D I S F ~ A \$ ~
6 7 7 0 \text { PAUSE}
6 7 8 0 \text { CLEAR}
6790 OUTPUT A ;"TRI GA.001 HS1"
6 8 0 0 ~ O U T P U T ~ A ~ ; " T C " '
6810 ENTER A ; C1,C2,C3,C4
6820 TRANSFER A TO X$ FHS
6830 DISP D里;"shows 'FASt dAtA'."
6840 DISP
6850 FOR J=0 TO 4
6860 IF INT(NUM(X$[8*J+1,8*J+1])/16)>9 THEN X(J)=9.99E99 @ GOTO 7070
6870 IF INT(NUM(X$[8*J+4,8*J+4])/16)>9 THEN X(J)=9.99E99@ G0TO 7070
6880 FOR I=1 T0 3
6890 R$[2*I-1,2*I-1]=CHR$(INT(NUM(X$[I+8*J,I+8*J])/16)+48)
6900 R$[2*I,2*I]=CHR$(BINAND(NUM(X$[I+8*J,I+8*J]),15)+48)
6910 NEXT I
6920 E=VAL(R末)
6930 FOR I=4 TO 6
6940 5$[2*I-7,2*I-7]=CHR$(INT(NUM(X$[I+8*J,I+8*J])/16)+48)
6950 5$[2*I-6,2*I-6]=CHR$(BINAND(NUM(X$[I+8*J,I+8*J]),15)+48)
6960 NEXT I
6970 B=UAL.(S$)
6980 C=NUM(X$[8*J+7,8*J+7])
6990 D=NUM (X$[8*J+8,8*J+6])
7000 IF C-C3<-4 THEN C=C+256
7010 IF D-Cl<-4 THEN D=D+256
7020 T=B+(C-CJ)/C4-(D-C1)/C2
7050 X(J)=E/T*10000000
7040 NEXT J
7050 DISP
7060 DISP F$
7070 PAUSE
7080 CLEAR
7090 DISP "Verify that the screen displays the time base frequency 5 times."
7100 DISF
7110 FOR J=0 TO 4
7120 DISP USING 7130 ; J+1,X(J)
7130 IMAGE 30,2X,"FREQUENCY = "D.DDDDDe," Hz"
7140 NEXT J
7150 DISP
7160 DISP F$
```

```
7170 PAUSE
7180 CLEAR
7190 DISP "Disconnect the BNC cable."
7200 DISP
7210 DISP B$
7 2 2 0 ~ P A U S E ~
7 2 3 0 ~ O U T P U T ~ A ~ ; " H S 0 ~ I N " ~
7240 GOTO 7960
7250 !
7260 ! END OF PROGRAM
7270 CLEAR
7280 DISP H$
7290 DISP
7300 DISP " CHECKPOINT RESULTS"
7310 DISP" FOR HP-IB ADDRESS";A
7320 DISP
7330 DISP H$
7340 IF C=2 THEN DISP @ GOTO 7380
7350 DISP
7360 DISP F$
7370 PAUSE
7380 CLEAR
7390 FOR I=1 TO 14
7400 IF R(I)=0 THEN R婁="NOT FERFORMED"
7410 IF R(I)=1 THEN R$="FAIL"
7420 IF R(I)=2 THEN R $="FASS"
7430 IF I=1 THEN DISP "CHECKPOINT ";I;" ";R$ @ GOTO 74G0
7440 IF I<10 THEN DISP " ";I;" ";R$ @ GOTO 7460
7450 DISP " ";I;R$
7460 NEXT I
7470 IF C=2 THEN DISP USING "5/" @ GOTO 7650
7480 DISP USING "#,K,/" ; F$
7490 PAUSE
7500 CLEAR
7510 DISP "Would you like a printed versionof the checkpoint results?"
7520 DISP
7530 DISP "Yes - Press Kl to receive a printed version."
7540 DISP
7550 DISP "No - Press k4 to proceed."
7560 ON KEY# 1,"YES" GOTO 7610
7570 OFF KEY# 3
7580 ON K'EY# 4," NO" GOTO 7670
7590 KEY LABEL
7600 GOTO 7600
7610 CLEAR
7620 CRT IS 2
7630 C=2
7640 GOTO 7270
7650 CRT IS I
7660 C=1
7670 LOCAL 7
7680 ABORTIO .7
```

```
7690 REWIND
7700 CLEAR
7710 DISP USING "5/"
7720 DISP H$
7 7 3 0 ~ D I S P
7740 DISP " END OF HP 5334A/B HP-IB"
7750 DISP " OPERATION UERIFICATION PROGRAM"
7760 DISP
7770 DISP H$
7780 END
7790 !
7800 !
7810 ! SUBROUTINE TO PRINT CHECKPOINT HEADINGS
7820 CLEAR
7 8 3 0 ~ D I S P ~ H \$ ~
7840 DISP
7850 DISP G$;S
7860 DISP I$
7 8 7 0 \text { DISP}
7880 DISP H$
7 8 9 0 ~ D I S P
7900 RETURN
7910!
7920 ! SUBPROGRAM TO TERMINATE CHECKPOINT EXECUTION
7930 DISP
7940 DISP F$
7950 PAUSE
7960 60SUB 7990
7970 G0SUB 8170
7 9 8 0 ~ G O T O ~ 8 4 2 0 ~
7990!
8000 ! SUBROUTINE TO PROMPT USERFOR CHECKPOINT RESULTS
8010 CLEAR
8020 DISP "Press the soft key correspondingto the results of this"
8030 DISP "checkpoint ...""
8040 DISP
8050 DISP "PASS - Press Kl to indicate that the 5334A/B passed."
8060 DISP
8070 DISP "FAIL - Press K4 to indicate that the 5334A/B failed."
8080 ON KEY# 1,"PASS" GOTO 8130
8090 OFF KEY# 3
8100 ON KEY# 4," FAIL" GOTO 8150
8110 KEY LABEL
8120 GOTO 8120
8130 R(S)=2
8140 RETURN
8150 R(S)=1
8160 RETURN
8170!
8180 ! SUBROUTINE TO DETERMINE NEXT PROGRAM STEP
8190 CLEAR
```

```
8200 DISP "Press a soft key to select the desimed checkpoint ..."
8210 DISP
8220 DISP "NEXT - Press Kl to perform the . next checkpoint."
8230 DISP
8240 DISP "REPEAT - Fress KJ to repeat this checkpoint."
8250 DISP
82G0 DISP "GOTO# - Press K4 to select an arbitrary checkpoint."
8270 ON KEY# 1,"NEXT" GOTO 8320
8280 ON KEY# 3." REPEAT" GOTO 8340
8290 ON KEY# 4," GOTO#" GOTO 8360
8300 KEY LABEL
8310 GOTO 8310
8320 D=S+1
8330 RETURN
8340 D=S
8350 RETURN
8360 CLEAR
8370 DISP "Enter checkpoint number desired ( 0 to 14), and press END LINE"
8380 DISP "(0 TERMINATES PROGRAM)."
8390 INPUT D
8400 IF D<0 OR D>14 THEN 8360
8410 RETURN
8420 !
8430 ! SUBPROGRAM TO BRANCH EXECUTION TO DESIRED CHECKPOINT
8440 IF D=0 THEN 7250
8450 IF D>7 THEN 8470
8460 ON D GOTO 1960,2270,2640,3050,3450,3800,4230
8470 ON D-7 GOTO 4430,4830,5170,5600,6140,6290,6630,7250
8480 !
8490 ! SUBROUTINE TO FROMT USER AND FAUSE
8500 DISP
8510 DISP A$
8520 PAUSE
8530 RETURN
8540
8550 ! SUBROUTINE TO BEEP AND WAIT 1.5 SECONDS
8560 BEEF 250,20
8570 WAIT 1500
8580 RETURN
8590
8600
8610 ! SUBROUTINE TO READ A STATUS BYTE
8620 M$="NO DATA READ"
8630 B=5POLL(A)
8640 WAIT 1000
8650 CLEAR
8660 DISP "The correct value for the status byte after reset is 16."
8670 DISP
8680 DISP "The returned value of the status byte is";B;"."
8690 IF B=16 THEN R=F*1
8700 IF B<>16 THEN F=R*D
8710 DISP
```


## Table 4-4. HP-IB Operational Verification

Program Listing (Continued)

```
8720 DISP F$
8 7 3 0 ~ P A U S E ~
8740 RETURN
8750 !
8760 ! SUBROUTINE TO INFORM USER THAT THE HP 85 HAS UERIFIED THE TEST
8770 CLEAR
8780 IF R=1 THEN GOTO 8830
8790 R(S)=1
8800 DISP "The HP 85 has verified that the 5334A/B failed this checkpoint."
8810 WAIT 3000
8 8 2 0 ~ R E T U R N
8830 R(S)=2
8840 DISP "The HP 85 has verified that the 5334A/B passed this checkpoint."
8 8 5 0 ~ W A I T ~ 3 0 0 0 ~
8860 RETURN
```


## SECTION 5 <br> ADJUSTMENTS

## 5-1. INTRODUCTION

5-2. This section provides the adjustments and checks for the Hewlett-Packard Model 5334B Universal Counter. With the exception of the 10 MHz Internal Oscillator Adjustment, these procedures should not be performed as routine maintenance but should be used: (1) after replacement of a part or component that may affect an adjustment, or (2) when the instrument fails the performance tests. Removal of the instrument top cover is required for most adjustments. Allow a 30 -minute warm-up prior to performing the adjustments.

5-3. Table 5-1 lists all of the adjustments by adjustment name, reference designation, adjustment paragraph, and description. Also included in this section are the adjustments for an HP 5334B equipped with the available options.

## 5-4. SAFETY CONSIDERATIONS

5-5. Although this instrument has been designed in accordance with international safety standards, this section contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition. Service adjustments should be performed only by a qualified service person.

## WARNING

ADJUSTMENTS IN THIS SECTION ARE PERFORMED WITH POWER SUPPLIED TO THE INSTRUMENT WHILE PROTECTIVE COVERS ARE REMOVED. THERE ARE VOLTAGES AT POINTS IN THE INSTRUMENT WHICH CAN, IF CONTACTED, CAUSE PERSONAL INJURY. BE EXTREMELY CAREFUL. ADJUSTMENTS SHOULD BE PERFORMED ONLY bY QUALIFIED SERVICE PERSONNEL WHO ARE AWARE OF THE HAZARDS INVOLVED (FOR EXAMPLE, FIRE AND ELECTRICAL SHOCK). WHERE MAINTENANCE CAN BE PERFORMED WITHOUT POWER APPLIED, THE INSTRUMENT SHOULD BE DISCONNECTED FROM ITS POWER SOURCE.

## NOTE

Use a nonmetallic adjustment tool whenever possible.

Table 5-1. Adjustable Components

| ADJUSTMENT NAME | REFERENCE DESIGNATION | ADJUSTMENT PARAGRAPH | DESCRIPTION |
| :---: | :---: | :---: | :---: |
| Power Supply | A1R123 | 5-12 | Sets the $\pm 3$ Volt Supply |
| DAC A/B Zero <br> (A ZERO) <br> ( B ZERO) | (A) A1R67 <br> (B) A1R85 | $\begin{aligned} & 5-13 \\ & 5-13 \end{aligned}$ | Sets DAC zero with no input |
| DAC A/B Gain (A GAIN) (B GAIN) | (A) A1R102 <br> (B) A1R103 | $\begin{aligned} & 5-14 \\ & 5-14 \end{aligned}$ | Sets DAC gain for correct voltage. |
| Internal Oscillator (Standard Oscillator) (Option 010) | $\begin{gathered} \text { A1C1 } \\ \text { "FREQ ADJ" } \end{gathered}$ | 5-15 | Maximizes accuracy of internal time base. |
| Channel A/B Offset (A VOS) <br> ( B VOS) | (A) A1R58, 132 <br> (B) A1R41, 133 | $\begin{aligned} & 5-16 \\ & 5-17 \end{aligned}$ | Sets Channel A/B sensitivity at 1 MHz . |
| Channel A/B MRC Input (CH A) (CH B) | (A) A1R130 <br> (B) A1R131 | $\begin{aligned} & 5-18 \\ & 5-19 \end{aligned}$ | Sets DC component of the MRC input signal. |
| Channel A/B <br> Attenuator <br> (CH A) <br> (CH B) | $\begin{aligned} & \text { A1C87 } \\ & \text { A1C89 } \end{aligned}$ | $\begin{aligned} & 5-20 \\ & 5-20 \end{aligned}$ | Sets attenuators for low freq applications. |
| Channel C Peak Detector (Option 030) | A1R328 | 5-21 | Sets Channel C sensitivity. |

## 5-6. EQUIPMENT REQUIRED

5-7. Table 1-5, of the Operating and Programming Manual, lists the equipment required for the adjustment procedures. If the test equipment recommended is not available, other equipment may be used if its performance meets the critical specifications listed in Table 1-5. The specified equipment required for each adjustment is referenced in each procedure.

## 5-8. FACTORY-SELECTED COMPONENTS

5-9. Factory-selected components are identified on the schematics and parts lists by an asterisk ( ${ }^{*}$ ) which follows the reference designator. The nominal value or range of the component is shown. Manual change sheets will provide updated information pertaining to selected components.

## 5-10. RELATED ADJUSTMENTS

5-11. Adjustments that interact are noted in the adjustment procedures. Table 5-1 lists the adjustment procedures and the recommended order of performance. Table 5-2, Post-Repair Adjustments, lists the recommended adjustments to perform following a repair to different sections of the Counter.

Table 5-2. Post-Repair Adjustments

| FUNCTIONAL BLOCK REPAIRED | SCHEMATIC SHEET | ADJUSTMENTS (paragraph) |
| :---: | :---: | :---: |
| Input Amplifier | Figure 8-20 | $5-16$ through 5-20 |
| DAC | Figure 8-21 | $5-13,5-14$ |
| Measurement | Figure 8-22 | None |
| Executive | Fone |  |
| HP-IB | Figure 8-22 | None |
| Time Base | Figure 8-24 | $5-15$ through 5-20 |
|  | (standard oscillator) | $5-15$ through 5-20 |
|  | Figures 8-24 and 8-27 | (Option 010) |
| Power Supply | Figure 8-24 | $5-12$ through 5-20 |
| Front Panel | Figure 8-28 | None |
| MATE (Option 700) | Figure 8-25 | $5-21$ |
| Channel C (Option 030) | Figure 8-26 |  |

## 5-12. POWER SUPPLY VOLTAGE ADJUSTMENT

Reference: Figure 8-24
Description: The +3 V dc power supply is adjusted for $+3.00 \mathrm{~V} \mathrm{dc} \pm .02 \mathrm{~V}$ dc at Test Point " +3 " using a digital multimeter.


Figure 5-1. +3 Volt Power Supply Adjustment Setup

## Equipment:

Digital Multitimeter (DMM) $\qquad$ HP 3468A

## Procedure:

1. Set the DMM as follows:
Function Vdc
Range AUTO
2. Connect DMM positive lead to TP5 ( +3 ), and connect the negative lead to "GND" Test Point.
3. Adjust A1R202 for a $D$ MM reading of $+3.00 \mathrm{~V} \mathrm{dc} \pm 0.02 \mathrm{~V} \mathrm{dc}$.


## 5-13. DIGITAL-TO-ANALOG CONVERTER (DAC) A/B ZERO ADJUSTMENT

Reference: Figure 8-21
Description: The zero reference positions for Channel A and B DAC trigger levels are set with no input signal.

HP5334B
UNIVERSAL COUNTER


Figure 5-2. DAC A/B Zero Adjustment Setup

Equipment:: None.

Procedure:

1. Set the HP 5334B as follows:

READ LEVELS $\qquad$ Voltage Peaks A (Press READ LEVELS twice)
2. Adjust A1R67 (A ZERO) for a 5334B front panel display of "0.00 0.00 A" Volts.
3. Set the HP 5334B as follows:

READ LEVELS $\qquad$ Voltage Peaks B
(Press READ LEVELS once)

4. Adjust A1R85 (B ZERO) for a 5334B front panel display of " 0.000 .00 b " Volts.

## 5-14. DIGITAL-TO-ANALOG CONVERTER (DAC) A/B GAIN ADJUSTMENT

Reference: Figure 8-21
Description: The voltage reference levels for the Channel A and and B DACs are set using a high resolution DC voltage input signal.


Figure 5-3. DAC A/B Gain Adjustment Setup

## Equipment:

DC Volt. Std.
FLUKE 343A

## Procedure:

1. Set the DC Standard as follows:

Output Voltage
$+5.000 \mathrm{~V} \mathrm{dc} \pm 0.001 \mathrm{~V}$
2. Set the HP 5334B as follows:

READ LEVELS
Voltage Peaks A
INPUT Impedance $1 \mathrm{M} \Omega$ ( $50 \Omega$ key LED off)
3. Connect the DC Standard to the HP 5334B Input A.
4. Adjust A1R102 (A GAIN) for a 5334B front panel display of $+5.00 \mathrm{~V} \mathrm{dc} \pm 0.02 \mathrm{~V}$ dc for both the positive and negative peaks.
5. Set the HP 5334B as follows:

READ LEVELS
Voltage Peaks B


INPUT Impedance ....................... $1 \mathrm{M} \Omega$ ( $50 \Omega$ key LED off)
6. Connect the DC Standard to the HP 5334B Input B.
7. Adjust A1R103 (B GAIN) for a 5334B front panel display of $+5.00 \mathrm{~V} \mathrm{dc} \pm 0.02 \mathrm{~V}$ dc for for both the positive and negative peaks.

## 5-15. 10 MHz REFERENCE OSCILLATOR FREQUENCY ADJUSTMENT

Description: The frequency of the internal 10 MHz oscillator time base is adjusted to a reference standard. The amplitude of the signal under test is also checked.

## NOTE

The following adjustment is for STANDARD EQUIPPED HP 5334Bs (without Option 010 Oven Oscillator).


Figure 5-4. Standard Oscillator Adjustment Setup

## Equipment:

Oscilloscope $\qquad$ HP 1715A (or equivalent)
Ref. Freq. Std 10 MHz

## Reference: Figure 8-24

## Procedure:

1. The HP 5334B should have been powered-up for at least 20 minutes prior to performing this adjustment.
2. Set the 5334B as follows:

FUNCTION.
FREQ A
GATE TIME
1 Second
TIME BASE INT (rear panel)
3. Connect the 10 MHz Frequency Standard to to the 5334 B


Input A.
4. Adjust A 1 C 1 (OSC ADJ) for a 5334 B front panel display of $10.000000 \mathrm{MHz} \pm 8 \mathrm{~Hz}$.
5. Set the oscilloscope as follows:
Channel A V/Div.
0.5 V

Time/Div..........................................0.05 S
Ch A Input Coupling...................... $50 \Omega$
Main Triggering ..............................INT
Internal Trigger............................... A
Vertical Display............................... A
Horizontal Display.......................... MAIN
6. Connect the 5334B TIME BASE output to the oscilloscope channel A input.
7. Verify that the signal is greater than 1.4 V p-p.

## NOTE

The following procedure is for the Option 010 Oven Oscillator equipped 5334B.


Figure 5-5. Option 010 Oscillator Adjustment Setup

Equipment:
Oscilloscope
HP 1715A (or equivalent)
Ref. Freq. Std 10 MHz

Reference: Figure 8-27


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## Procedure:

1. Allow the ovenized oscillator a 24 -hour warm-up period prior to performing this adjustment. The crystal oscillator oven is operating whenever the instrument is connected to its power source.
2. Set the oscilloscope as follows:

Channel A V/Div. ...........................0.5V
Time/Div...........................................0.01 $\mu \mathrm{s}$
Ch A Input Coupling...................... $50 \Omega$
Main Triggering .............................EXT
Vertical Display...............................A
Horizontal Display.......................... MAIN
3. Set the 5334 B as follows:

FUNCTION....................................FREQ A
GATE TIME................................... 1 Second
TIME BASE....................................INT (rear panel)
4. Connect the 10 MHz Frequency Standard to the oscilloscope External Trigger input.
5. Connect the TIME BASE output to the oscilloscope channel $\mathbf{A}$ input.
6. Adjust the "FREQ ADJ" pot on the Option 010 Oven Oscillator until the scope pattern does not move sideways more than 1 division in 10 seconds.
7. Set the oscilloscope as follows:

Main Triggering ............................. INT
Internal Trigger............................... A
Channel A Input Coupling............ $50 \Omega$
8. Connect the 5334B TIME BASE output to the oscilloscope channel A input.
9. Verify that the signal is greater than 1.4 V p-p.

## 5-16. CHANNEL A SENSITIVITY OFFSET ADJUSTMENT

Reference: Figure 8-20 and 8-21
Description: The sensitivity of the Channel A Input is adjusted using a 1 MHz input signal (interactive adjustment).


Figure 5-6. Channel A Sensitivity Adjust Setup

## Equipment:

Function Generator ....................... HP 3325A

## Procedure:

1. Set the function generator as follows:

Frequency 1 MHz
Function Sine Wave
Amplitude 8 mV rms
2. Set the 5334B as follows:

FUNCTION.
FREQ A
SENS (blue key) ON
CHAN A SENS Control................MAX
INPUT A $50 \Omega$.................................ON
GATE TIME 1 Second

3. Adjust A1R58 (A VOS) to the mid-range position, and adjust A1R132 to the fully counterclockwise position. A1R132 is set to maximum sensitivity for Channel $A$ in this position.
4. Connect the function generator signal to the 5334B Input A. Connect Time Base as shown in Figure 5-6.
5. Adjust A1R58 (A VOS) for a 5334B front panel display of $1.00000000 \mathrm{MHz} \pm 0.06 \mathrm{~Hz}$.
6. Decrement the function generator signal amplitude by 1 mV rms and repeat step 5.

Continue to repeat steps 5 and 6 until no further adjustment can be made because the signal level drops below the Counter's sensitivity limit (indicated by the GATE LED staying on continuously and no display update or an inaccurate reading).
7. Set the function generator amplitude to 6.5 mV rms.
8. Adjust A1R132 to the point at which the 5334B stops counting and then carefully adjust A1R132 so the 5334B just starts counting and accurately displays $1.00000000 \mathrm{MHz} \pm 0.06 \mathrm{~Hz}$.
9. Set the function generator amplitude to 4 mV rms.
10. Verify that the 5334 B does not count the 1 MHz signal.

If the 5334 B is able to count at 4 mV rms , set the function generator amplitude to 7 mV rms and repcat steps 8,9 , and 10 . If necessary, step 8 can be performed at 7.5 or 8.0 mV rms so that there is no count at 4 mV rms.

NOTE
Do not adjust A1R132 to a level above 8 mV rms. If the setting is made at 8 mV rms and the 5334B still counts at 4 mV rms, a problem exists in the Input Amplifier circuitry.

## 5-17. CHANNEL B SENSITIVITY OFFSET ADJUSTMENT

Reference: Figure 8-20 and 8-21
Description: The sensitivity of the Channel B Input is adjusted using a 1 MHz input signal (interactive adjustment).


Figure 5-7. Channel B Sensitivity Adjust Setup

## Equipment:

Function Generator
HP 3325A

## Procedure:

1. Set the function generator as follows:

Frequency
1 MHz
Function Sine Wave
Amplitude 8 mV rms
2. Set the 5334 B as follows:

| FUNCTI | FREQ B |
| :---: | :---: |
| SENS (blue key).......... | ON |
| CHAN B SENS Control. | MAX |
| INPUT B 50ת................. | ON |
| GATE TIME. | 1 Second |


3. Adjust A1R41 (B VOS) to the mid-range position, and adjust A1R133 to the fully counterclockwise position. A1R133 is set to maximum sensitivity for Channel $B$ in this position.
4. Connect the function generator signal to the 5334B Input B. Connect Time Base as shown in Figure 5-7.
5. Adjust A1R41 (B VOS) for a 5334 B front panel display of $1.00000000 \mathrm{MHz} \pm 0.06 \mathrm{~Hz}$.
6. Decrement the function generator signal amplitude by 1 mV rms and repeat step 5 .

Continue to repeat steps 5 and 6 until no further adjustment can be made because the signal level drops below the Counter's sensitivity limit (indicated by the GATE LED staying on continuously and no display update or an inaccurate reading).
7. Set the function generator amplitude to 6.5 mV rms.
8. Adjust A1R133 to the point at which the 5334B stops counting and then carefully adjust A1R133 so the 5334B just starts counting and accurately displays $1.00000000 \mathrm{MHz} \pm 0.06 \mathrm{~Hz}$.
9. Set the function generator amplitude to 4 mV rms .
10. 10. Verify that the 5334 B does not count the 1 MHz signal.

If the 5334 B is able to count at 4 mV rms , set the function generator amplitude to 7 mV rms and repeat steps 8,9 , and 10 . If necessary, step 8 can be performed at 7.5 or 8.0 mV rms so that there is no count at 4 mV rms.

## NOTE

Do not adjust A1R133 to a level above 8 mV rms. If the setting is made at 8 mV rms and the 5334B still counts at 4 mV rms, a problem exists in the Input Amplifier circuitry.

## 5-18. MULTIPLE-REGISTER COUNTER (MRC) INPUT ADJUSTMENT, CH A

Reference: Figure 8-20
Description: The Channel A DC biasing level on the MRC input signal is optimized at two frequencies on both the positive and negative slopes of the signal (interactive adjustment).


Figure 5-8. MRC Input Adjust/Channel A Setup

## Equipment:

Signal Generator $\qquad$ HP 8656B

## Procedure:




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## NOTE

For 5334B instruments equipped with Option 060, set Signal Generator amplitude to $40.0 \mathrm{mV} \pm 0.4 \mathrm{mV}$. Terminate the unused Channel $A$ and $B$ rear inputs with $50 \Omega$ loads.
2. Set the 5334 B as follows:

FUNCTION
FREQ A
SENS (blue key)...........................ON
INPUT A SENS Control...............MAX
INPUT A $50 \Omega$..............................ON
GATE TIME............................... 1 Second
INPUT A SLOPE OFF (positive)
3. Connect the Signal Generator output to the 5334B Input A. Connect Time Base as shown in Figure 5-8.
4. Adjust A1R130 (CH A) for a 5334B front panel display of $70.000000 \mathrm{MHz} \pm 4 \mathrm{~Hz}$ at both the positive and negative slope settings.
5. Decrement the Signal Generator amplitude by 3 mV rms.
6. Adjust A1R130 (CH A) for a 5334B front panel display of $70.000000 \mathrm{MHz} \pm 4 \mathrm{~Hz}$ at both the positive and negative slope settings. If this adjustment is not possible because the signal level has dropped below the Counter's sensitivity limit, go to step $\mathbf{1 0}$. Otherwise, continue on to step 7.
7. Set the Signal Generator frequency to 104 MHz .
8. Adjust A1R130 (CH A) for a 5334 B front panel display of $104.000000 \mathrm{MHz} \pm 4 \mathrm{~Hz}$ at both the positive and negative slope settings. If this adjustment is not possible, go to step 10 . Otherwise continue on to step 9 .
9. Set the Signal Generator frequency to 70 MHz and repeat steps 5 through 9 until adjustment is no longer possible and this loop is exited from step 6 or 8.
10. Increment the Signal Generator amplitude in 0.3 mV rms steps until Counter displays a stable frequency count.
11. Set the Signal Generator frequency to 104 MHz .
12. Adjust A1R130 (CH A) for a 5334B front panel display of $104.000000 \mathrm{MHz} \pm 4 \mathrm{~Hz}$ at both the positive and negative slope trigger settings. If this adjustment is not possible, repeat steps 10 through 12 until this adjustment is completed and then continue with step 13.
13. Set the Signal Generator frequency to 70 MHz .
14. Adjust A1R130 (CH A) for a 5334 B front panel display of $70.000000 \mathrm{MHz} \pm 4 \mathrm{~Hz}$ at both the positive and negative slope settings. If this adjustment is not possible, repeat steps 10 through 14 until this adjustment is completed and then continue with step 15.
15. Set the Signal Generator frequency to 70 MHz and the amplitude to $28.0 \mathrm{mV} \pm 0.3 \mathrm{mV}$.

## NOTE

For 5334B instruments equipped with Option 060, set Signal Generator amplitude to $40.0 \mathrm{mV} \pm 0.4 \mathrm{mV}$.
16. Verify that the 5334 B front panel displays $70.000000 \mathrm{MHz} \pm 4 \mathrm{~Hz}$ at both the positive and negative slope settings.
17. Set the Signal Generator frequency to 104 MHz and the amplitude to $28.0 \mathrm{mV} \pm 0.3 \mathrm{mV}$.

## NOTE

For 5334B instruments equipped with Option 060, set Signal Generator amplitude to $40.0 \mathrm{mV} \pm 0.4 \mathrm{mV}$.
18. Verify that the 5334 B front panel displays $104.000000 \mathrm{MHz} \pm 4 \mathrm{~Hz}$ at both the positive and negative slope settings.

## 5-19. MULTIPLE-REGISTER COUNTER (MRC) INPUT ADJUSTMENT, CH B

Reference: Figure 8-20
Description: The Channel B DC biasing level on the MRC input signal is optimized at two frequencies on both the positive and negative slopes of the signal (interactive adjustment).


Figure 5-9. MRC Input Adjust/Channel B Setup

## Equipment:

Signal Generator HP 8656B

## Procedure:

1. Set the Signal Generator as follows:
Frequency
70 MHz
Amplitude
$28.0 \mathrm{mV} \pm 0.3 \mathrm{mV}$

## NOTE

For 5334B instruments equipped with Option 060, set Signal Generator amplitude to $40.0 \mathrm{mV} \pm 0.4 \mathrm{mV}$. Terminate the unused Channel $A$ and $B$ rear inputs with $50 \Omega$ loads.
2. Set the 5334 B as follows:

FUNCTION.
FREQ B
SENS (blue key). ON
INPUT B SENS Control...............MAX
INPUT B $50 \Omega$ ON
GATE TIME.
1 Second
INPUT B SLOPE $\qquad$ OFF (positive)

3. Connect the Signal Generator output to the 5334B Input B. Connect Time Base as shown in Figure 5-9.
4. Adjust A1R131 (CH B) for a 5334B front panel display of $70.000000 \mathrm{MHz} \pm 4 \mathrm{~Hz}$ at both the positive and negative slope settings.
5. Decrement the Signal Generator amplitude by 3 mV rms.
6. Adjust A1R131 (CH B) for a 5334B front panel display of $70.000000 \mathrm{MHz} \pm 4 \mathrm{~Hz}$ at both the positive and negative slope settings. If this adjustment is not possible because the signal level has dropped below the Counter's sensitivity limit, go to step 10 . Otherwise continue on to step 7.
7. Set the Signal Generator frequency to 104 MHz .
8. Adjust A1R131 (CH B) for a 5334 B front panel display of $104.000000 \mathrm{MHz} \pm 4 \mathrm{~Hz}$ at both the positive and negative slope settings. If this adjustment is not possible, go to step 10 . Otherwise continue on to step 9 .
9. Set the Signal Generator freqency to 70 MHz and repeat steps 5 through 9 until adjustment is no longer possible and this loop is exited from step 6 or 8 .
10. Increment the Signal Generator amplitude in 0.3 mV rms steps until Counter displays a stable frequency count.
11. Set the Signal Generator frequency to 104 MHz .
12. Adjust A1R131 (CH B) for a 5334 B front panel display of $104.000000 \mathrm{MHz} \pm 4 \mathrm{~Hz}$ at both the positive and negative slope settings. If this adjustment is not possible, repeat steps 10 through 12 until this adjustment is completed and then continue with step 13.
13. Set the Signal Generator frequency to 70 MHz .
14. Adjust A 1 R 131 (CH B) for a 5334 B front panel display of $70.000000 \mathrm{MHz} \pm 4 \mathrm{~Hz}$ at both the positive and negative slope settings. If this adjustment is not possible, repeat steps 10 through 14 until this adjustment is completed and then continue with step 15.
15. Set the Signal Generator frequency to 70 MHz and amplitude to $28.0 \mathrm{mV} \pm 0.3 \mathrm{mV}$.

## NOTE

For 5334B instruments equipped with Option 060, set Signal Generator amplitude to $40.0 \mathrm{mV} \pm 0.4 \mathrm{mV}$.
16. Verify that the 5334 B front panel displays $70.000000 \mathrm{MHz} \pm 4 \mathrm{~Hz}$ at both the positive and negative slope settings.
17. Set the Signal Generator frequency to 104 MHz and the amplitude to $28.0 \mathrm{mV} \pm 0.3 \mathrm{mV}$.

## NOTE

For 5334B instruments equipped with Option 060, set Signal Generator amplitude to $40.0 \mathrm{mV} \pm 0.4 \mathrm{mV}$.
18. Verify that the 5334 B front panel displays $104.000000 \mathrm{MHz} \pm 4 \mathrm{~Hz}$ at both the positive and negative slope settings.

## 5-20. ATTENUATOR ADJUSTMENT

## Reference: Figure 8-20

Description: The Channel A and B attenuators are adjusted for low frequency applications.


Figure 5-10. Attenuator Adjustment Setup

## Equipment:

Oscilloscope HP 1715A (or equivalent)
Function Generator HP 3325A

## Procedure:

1. Set the oscilloscope as follows:
Channel A V/Div 0.01 V

Time/Div..................................................... 0.1 ms
Channel A Coupling.....................AC
Main Triggering .............................INT
Internal Trigger............................A
Vertical Display............................A
Horizontal Display. MAIN
2. Set the function generator as follows:

Frequency.
1 kHz
Function
Square Wave
Amplitude $6 \mathrm{~V}-\mathrm{p} \pm 0.3 \mathrm{~V}$
3. Set the 5334B as follows:

FUNCTION.
FREQ A
SENS (blue key)............................. ON
CH A \& B SENS Controls........... MAX
COM A.......................................ON
CHANNEL A AND B
X10 ATTENUATORS ON
4. Connect the function generator output to the 5334B Input A.
5. Using a calibrated $10: 1$ oscilloscope probe, connect the oscilloscope Channel A to A1R55 (A end).

## NOTE

Calibrated here means simply checking the probe against the oscilloscope front panel calibration signal. Display the calibration signal on the scope CRT and adjust probe tuning capacitor, if necessary, for a correctly attenuated by 10 signal.
6. Adjust A1C87 to obtain an ideal square wave on the oscilloscope display. Adjust out any overshoot visible on the waveform. (Be careful not to back adjustment screw out entirely.) See Figure 5-11 for an example of overshoot.
7. Connect the oscilloscope probe to A1R38 (B end).
8. Adjust A1C89 to obtain an ideal square wave on the oscilloscope display. Adjust out any overshoot visible on the waveform. (Be careful not to back screw out entirely.) See Figure 5-11 for an example of overshoot.


Figure 5-11. Square Wave Overshoot

## 5-21. CHANNEL C PEAK DETECTOR ADJUSTMENT, OPTION 030

Reference: Figure 8-26
Description: The input sensitivity of Channel C is adjusted.


Figure 5-12. Option 030 Channel C Peak Detector Adjust Setup

Equipment:



[^0]
## NOTE

The 10 dB attenuator is used here for impedance matching.

## Procedure:

1. Connect the Signal Generator output to the Power Sensor/Power Meter as shown in Figure 5-12.
2. Set the Signal Generator output Frequency to 990 MHz .
3. While observing the display on the HP 436A Power Meter, adjust the amplitude of the output signal for a power reading of $-30.73 \mathrm{dBm} \pm 0.1 \mathrm{dBm}$, which is equivalent to $6.5 \mathrm{mV} \mathrm{rms} \pm 0.12 \mathrm{mV}$. If your $\mathbf{H P} 5334 \mathrm{~B}$ has Option 60, rear panel inputs, then adjust the amplitude for a power $29.73 \mathrm{dBm} \pm 0.1 \mathrm{dBm}$ (equivalent to $7.3 \mathrm{mV} \mathrm{rms} \pm 0.12 \mathrm{mV}$ ).
4. Now, connect the Signal Generator output to the 5334B's INPUT C through the HP 8491A 10 dB attenuator as shown in Figure 5-12.
5. Connect the Time Base Out of the 5334B to the Time Base In of the Signal Generator as shown in Figure 5-12.
6. Set the 5334B as follows:

FUNCTION.....................................FREQ C
GATE TIME..................................1.3 Seconds

## CAUTION

For 5334Bs containing A1 Main Boards that are Revision C and below, take the following precaution:

In the next step (7), R319 (10 ohm resistor) will short out, if R328 is left too long in its fully clockwise position. To prevent this, quickly perform steps 7 and 8.
7. Adjust R328 fully clockwise.
8. Adjust R328 counter clockwise until the 5334B just starts to gate (GATE LED will flash).
9. Verify that the 5334B front panel displays $990.000000 \mathrm{MHz} \pm 2 \mathrm{~Hz}$.

This concludes the Channel C Peak Detector Adjustment.

## SECTION 6 REPLACEABLE PARTS

## 6-1. INTRODUCTION

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the part list and throughout this manual. Table $6-2$ lists all replaceable parts for the 5334B in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturer's code numbers.

## 6-3. ABBREVIATIONS

6-4. Table 6-1 lists abbreviations used in the parts list, schematics, and throughout this manual. In some cases, two forms of the abbreviation are used, one all in capital letters, and one partial or no capitals. This occurs because abbreviations in the parts list are always capitals. However, in the schematics and other parts of this manual, other abbreviation forms are used with both lower and upper case letters.

Table 6-1. Reference Designations and Abbreviations

## REFERENCE DESIGNATIONS



## 6-5. REPLACEABLE PARTS

6-6. Table 6-2 is the list of replaceable parts, and is organized as follows:
a. Electrical assemblies and their components in alphanumeric order by reference designation.
b. Chassis-mounted parts in alphanumeric order by reference designation.
c. Miscellaneous parts.

6-7. The information given for each part consists of the following:
a. Hewlett-Packard part number.
b. Part number check digit (CD).
c. Total quantity (QTY) used in the instrument.
d. Part description.
e. Five-digit code that represents a typical manufacturer.
f. Manufacturer's part number.

## NOTE

The total quantity for each part used in an assembly is given only once at the first appearance of the part number in the list.

## 6-8. ILLUSTRATED PARTS BREAKDOWN

6-9. Most mechanical parts are identified in Figure 6-1. This figure is located at the end of the replaceable parts table.

## 6-10. ORDERING INFORMATION

6-11. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are:
a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.
b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).
c. Prepaid transportation (there is a small handling charge for each order).
d. No invoices - to provide these advantages, a check or money order must accompany each order.

6-12. Mail order forms and specific ordering information is available through your local HP office. Addresses and phone numbers are located at the back of this manual.

6-13. To order a part that is not listed in the replacement parts tables, include the instrument model number, instrument serial number, the description and function of the part, and the number of parts required.

Table 6-2. Replaceable Parts


See introduction th this section for ordering information
*indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

| Reference Designation | HP Part Number | $\left\|\begin{array}{l} C \\ D \end{array}\right\|$ | Qty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A1C66 | -160-45,57 | 0 |  | CAPACITOR-FXO . IUF +-20\% 50VOC CER | 16299 | CACO4×7P104MO50A |
| A1CE 7 | 0160-4554 | 7 |  | CAPACITCR-FXD . O1UF +-20\% SOVDC CEP | 29480 | 0160-4554 |
| A1C68 | 0160-46.54 | 7 |  | CAPACITOP-FXO . OLUF +-20\% 50VOC CEP | : 4. | -1 1 0-4554 |
| A1CE9 | 0160-45,54 | 7 |  | CAPACITOR-FXD . OJUF +-20\% SOVIT CEP | 34\%. | (1160-4554 |
| 41070 | 0160-4788 | 7 |  | CAPACIITOP-FXD 27PF +-5\% 100VI EP 0+-30 | 28480 | $0160-4785$ |
| A1. $\cdot$ | 0160-45. | 0 |  |  | 16299 | CAC04×7P104MÚ50A |
| A1. 12 | 0160-45.57 | 0 |  | CAPACITOR-FXD . 1UF - 20\% 50VDC CER | 16299 | CACO4×7P104MOSOA |
| A1C73 | $0160-455$ | 0 |  | CAPACITOR-FXD . $1 \mathrm{UF}+20 \% 50 \mathrm{VOC}$ CEP | 18299 | CAC04×7P104M050A |
| $41 C 74$ | 0160-4387 |  | 2 | CAPACITOR-FXD 47PF +-5\% 200vDC CER $0+30$ | 28480 | 0160-4387 |
| A1C75 | 0160-3879 | 7 |  | CAPACITOR-FXD . OIUF +-20\% 100VOC CEP. | 28480 | 0160.3879 |
| A1c.76 | 0160-4387 | 4 |  | CAPACITOP FXD 47PF +-5\% 200VDC CEP O+-30 | 28480 | 0160-4387 |
| A1C77 | 0160-4554 | 7 |  | CAPACITOR-FXD . OIUF +-20\% SOVDC CER | 28480 | 0160-4554 |
| A1C7\% | 0160-4554 | 7 |  | CAPACITOR-FXD . O1UF +-20\% 50VOC CER | 28480 | 0160-4554 |
| AlC79 | $0: 000-4371$ | 6 |  | CAPACITOR-FXD 680PF +-5\% 100VOC CER | 28480 | 0160.4371 |
| AlC80 | 0160-0576 | 5 |  | CAPACITOR-FXD . $1 \mathrm{UF}+$ +2n\% 50 VOC CER | 28480 | 0160-0576 |
| AlC81 | 0160-4? ${ }^{\text {a }}$ ( | 3 | 1 | CAPACITOR-FXD 15PF +-5\% . 00 V CER COG | 28480 | (1160-4386 |
| A1C82 Alc8? |  |  |  | NOT ASSIGNED |  |  |
| Alc8? | 0160-05.76 | 5 |  | 1.APACITOR-FXD . 1UF +-20\% 50VDC CER | 28480 | $0160 \cdot 0576$ |
| Alc84 | 01604.57 | 0 |  | CAPACITOR-FXD. 1UF +-20\% SOVOC CER | 16299 | CAC04×7R104M0SOA |
| A1C85 | 01604557 | 0 |  | CAPACITOR FXX . IUF +-20\% 50VDC. CER | 16299 | CAC04×7R104M050A |
| A1C86 | 0160-4554 | 7 |  | CAPACITOR-FXD . O1UF +-2U\% 50VOC CER | 28480 | 0160-4554 |
| A1C87 | 0121-0168 | 9 | 2 | CAPACITOR-V TRMPSTN .2-1.5PF 600V | 28480 | 0121-0168 |
| A 11688 | 0160-4527 | 4 | 1 | CAPACI TOR-FXO 56PF +-5\% 200V CEP COG | 06352 | FD12COG20560J |
| A1C89 | 0121-0168 | 9 |  | TAPACITOR-V TRMPSTN . 2-1.5PF 600V | 28480 | $0121-0168$ |
| A1C90 | 0160-4554 | 7 |  | CAPACITOR-FXD . O1UF +-20\% SOVDC CER | 28480 | 0160-4554 |
| A1C91 | 0160-4554 | 7 |  | CAPACITOR-FXD . O1UF +-20\% SOVOC CER | 28480 | 0160-4554 |
| A1C92 | 0160-3879 | 7 |  | CAPACITOR-FXD . O1UF +-20\% 100VDC CER | 28480 | 0160-3879 |
| A1C93 | 0160-4554 | 7 |  | CAPACITOR-FXD . O1UF +-20\% SOVDC CER | 28480 | 0160-4554 |
| A1C94 | 0160-45,54 | 7 |  | CAPACITOR-FXD . DIUF +-20\% SOVDC CER | 28480 | 0160-4554 |
| Alc95 | 0160-5108 | 9 | 2 | CAPACITOR-FXD . O1UF +-10\% 500VDC CER | 28480 | 0160-5108 |
| Alc96 | 0160-4554 | 7 |  | CAPACITOR-FXD . O1UF +-20\% 50VDC CER | 28480 | 0160-4554 |
| Alc97 | 0160-5108 | 9 | 2 | CAPACITOR-FXD. O1UF + $10 \%$ 500VOC. CER | 28480 | 0160-5108 |
| Alc98 | 0180-4786 | 7 |  | CAPACITOR-FXD 27PF +-5\% 100VDC CER 0+-30 | 28480 | $0160-4785$ |
| A1C93 | 0160-4791 | 4 |  | CAPACITOR-FXD 10PF +-5x 100VOC CER 0+-30 | 28480 | 0160-4791 |
| A1C100 | 0160-4554 | 7 |  | CAPACITOR-FXD . OIUF +-20\% SOVDC CER | 28480 | 0160-4554 |
| AlCl01 |  |  |  | NOT ASSIGNED |  |  |
| AlCl02 |  |  |  | NOT ASSIGNED |  |  |
| Alcio3 | 0180-3375 | 0 | 1 | CAPACITOR-FXD 3300UF +30-10\% 16VDC AL | 28480 | 0180-3375 |
| A1C104 | 0160-0576 | 5 |  | CAPACITOR-FXD. $14 \mathrm{~F}+-20 \%$ 50VDC CER | 28480 | 0160-0576 |
| A1C105 | 0160-4554 | 7 |  | CAPACITOR-FXO . O1UF +-20\% SOVDC CER | 28480 | 0160-4554 |
| ${ }^{\text {AlC106 }}$ | 0160-4554 | 7 |  | CAPACITOR-FXD . D1UF +-20\% SOVDC CER | 28480 | 0160-4554 |
| $\begin{aligned} & \text { A1C107- } \\ & \text { A1C2000 } \end{aligned}$ |  |  |  | NOT ASSIGNED |  |  |
| A1C201 | 0180-4076 |  | 4 | CAPACITOR-FXD 4700UF + $30-10 \% 35 \mathrm{~V}$ ELECT | 04200 | 80D472P035JC5AD2089 |
| A1C202 | 0180-4076 | 0 |  | CAPACITOR-FXD 4700UF $+30-10 \%$ 35VDC ELECT | 04200 | 80D472P035JC50A02089 |
| A1C203 | 0180-4076 | 0 |  | CAPACITOR-FXD 4700UF $+30-10 \%$ 35VDC ELECT | 04200 | 80D472P035JC50AD2089 |
| A1C204 | 0180-4076 | 0 |  |  | 04200 | 80D472P035JC50A02089 |
| AlC205 |  |  |  | NOT ASSIGNED |  |  |
| A1C206 |  |  |  | NOT ASSIGNED |  |  |
| A1C207 | 0160-4065 | 5 | 2 | CAPACITOR-FXD . $1 \mathrm{LJF}+-20 \%$ 250VAC(RMS) | 28480 | 0160-4065 |
| A1C208 | 0160-4281 | 7 | 2 | CAPACITOR-FXD 2200PF +20\% 250VAC(RMS) | C0633 | PME271Y422 |
| A1C209 | 0160-4281 | 7 |  | CAPACITOR-FKD 2200PF +20\% 250VAC(RMS) | C0633 | PME271Y422 |
| A1C210 | 0160-4065 | 5 |  | CAPACITOR-FXD . IUF +-20\% 250VAC(RMS) | 28480 | 0160-4065 |
| A1C211 | 0180-4136 | 3 | , | CAPACITOR-FXD 10UF +-10\% 20 V TA | 04200 | $1730106 \times 9020 \mathrm{~W}$ |
| A1C212 | 0180-3831 | 3 | 2 | CAPACITOR-FXD 10UF +-10\% 35VDC TA | 56289 | $2990106 \times 9035081$ |
| A1C213 | 0180-3775 | 4 |  | CAPACITOR-FXD G8UF +-20\% 10VDC TA | $2848{ }^{1}$ | 0180-3775 |
| A1C214 | 0180-3775 | 4 |  | CAPACITOR-FXD 68UF +-20\% 10VOC TA | 28480 | 0180-3775 |
| A1C215 | 0180-3775 | 4 |  | CAPACITOR-FXD 68UF +-20\% 10VDC TA | 28480 | 0180-3775 |
| A1C216 | 0180-3775 | 4 |  | CAPACITOR-FXO G8UF +-20\% lovor TA | 28480 | 0180-3775 |
| A1C217 | 0180-3775 | 4 |  | CAPACITOR-FKC 68UF +-20\% 10VOC TA | 28480 | (1180-3775 |
| Alc218 | 0180-3775 | 4 |  | CAPACITOR-FXD G8UF +-20\% 10VDC TA | 28480 | 0180-3775 |
| A1C219 | 0150-3775 | 4 |  | CAPACITOP-FXD ESUF +-20\% 10VOC TA | 28480 | 0180-3775 |
| A1C220 | 0180-3775 | 4 |  | CAPACITOR-FXD 68UF +-20\% 10VDC TA | 28480 | 0180-3775 |
| A1C2, 1 | 0:80-3775 | 4 |  | CAPACITOR-FXD G8UF +-20\% 10VOC TA | 28480 | 0180-3775 |
| A10'22 | 0180-3775 | 4 |  | CAFACITOR-FXD G8UF +-20\% 10VDC TA | 28480 | 0180-3775 |
| Allais | 0130-3775 | 4 |  | CAPACITOR-FXD 68UF +-20\% 10VO ${ }^{-1}$ | 28480 | 0180-3775 |
| A1C224 | 0180-3775 | 4 |  | CAPACITOP-FXC E8UF +-20\% luvac in | 28480 | 0180-3775 |
| A1C225 | 018i-3775 | 4 |  | CAPACITOP-FXD G8UF +-20\% lovDC IA | 28480 | 11180-3775 |

Table 6-2. Replaceable Parts (Continued)

| Reference Designation | HP Part Number | $\begin{aligned} & C \\ & D \end{aligned}$ | Qty | Description | Mir Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A1C226 | 0180-3775 | 4 |  | CAPACIIOP-FXD 68UF +-20\% 10VDC TA | 28480 | 01803775 |
| A1C227 | 0160-4557 | 0 |  | CAPACITOR-FXD . IUF +-20\% 50VUC CER | 16299 | CACO4X7R104M050A |
| A1C228- |  |  |  | NOT ASSIGNED |  |  |
| A1C291 | 0160-480\% | 4 | 1 | CAPACITOR-FXD 470PF +-5\% 100VDC CEP. | 2848: | 0160-4808 |
| A1C292 | 0180-02\% | 0 | 2 | CAPACIIOR-FXI 1UF +-21\% SOVDC TA | 56285 | $1500105 \times 0050 A^{2}$ |
| A1C293 | 0180-455. | 0 |  | CAPACITOR-FXD .1UF + $0 \%$ SOVDC CEP | 16294 | - ACO4×7R104M050A |
| A1C294 | 0180-0230 | 0 |  | CAPACITOR-FXD 1UF + $20 \% 50 \mathrm{~V}$ TA | 04200 | 150D105 $\times 0050 \mathrm{~A} 2 \mathrm{DYS}$ |
| A1C300 |  |  |  | NOT ASSIGNED |  |  |
| AlC301 | 0160-0576 | 5 |  | CAPACITOR-FXD .1UF +-20\% 50VDC CER | 28480 | 0160-0576 |
| AlC302 | 0150-0576 | 5 |  | CAPACITOR-FXD. 1UF +-20\% 50VDC CER | 28480 | 0160-0576 |
| A1C303 | 0160-0576 | 5 |  | CAPACITOR-FXD. 1UF +-20\% 50VDC CER | 28480 | 0160-0576 |
| A1C304 | 0160-0576 | 5 |  | CAPACITOR-FXD 1UF +-20\% 50VDC CER | 28480 | 0160-0576 |
| A1C305 | 0160-4046 | 6 | 8 | CAPACITOR-FXD 1000PF +-5\% 10DVDC CER | 28480 | 0160-4040 |
| A1C306 |  |  |  | NOT ASSIGNED |  |  |
| A1C307 | 0160-0576 | 5 |  | CAPACITOR-FXD .1UF +-20\% 50VDC CER | 28480 | 0160-0576 |
| A1C308 | 0160-4040 | 6 |  | CAPACITOR-FXD 1000PF +-5\% 100VDC CER | 28480 | 0160-4040 |
| ${ }^{\text {A } 1,309}$ | 0160-4040 | $\varepsilon$ |  | CAPACITOR-FXD 1000PF +-5\% 100VDC CER | 28480 | 01604040 |
| Alc310* | 0160-4382 | 9 | 1 | CAPACITOR-FXO 3.3PF +-. 25PF 200VDC CER | 28480 | 0160-4382 |
| A1C311 | 0160-0576 | 5 |  | CAPACITOR-FXD . 1JF +-20\% 50VDC CER | 28480 | 0160-0576 |
| A1C312 | 0160-0576 | 5 |  | CAPACITOR-FXD . 1UF +-20\% SOVDC CER | 28480 | 0160-0576 |
| A1C313 | 0160-4040 | ${ }_{6}$ |  | CAPACITOR-FXD 1000PF +-5\% 100VDC CER | 28480 | 0160-4040 |
| A1C314 | 0160-0576 | 5 |  | CAPACITOR-FXD . $1 \mathrm{UF}+-20 \%$ SOVDC CER | 28480 | 0160-0576 |
| A1C315 | 0160-0576 | 5 |  | CAPACITOR-FXD . 1UF +-20\% 50VDC CER | 28480 | 0160-0576 |
| A1c316 | 0160-0576 | 5 |  | CAPACITOR-FXD . 1UF +-20\% 50VDC CER | 28480 | 0160-0576 |
| A1C317 | 0160-4040 | 6 |  | CAPACITOR-FXD 1000PF +-5\% 100VDC CER | 28480 | 0160-4040 |
| A1C318 | 0160-0576 | 5 |  | CAPACITOR-FXD. 1UF +-20\% SOVDC CER | 28480 | 0160-0576 |
| A1C319 | 0160-0576 | 5 |  | CAPACITOR-FXD . 1 UF +-20\% 50VDC CER | 28480 | 0160-0576 |
| A) C 320 | 0160-4040 | 6 |  | CAPACITOR-FXD 1000PF +-5\% 100VDC CER | 28480 | 0160-4040 |
| A1C321 | 0160-0576 | 5 |  | CAPACITOR-FXD . 1UF +-20\% SOVOC CER | 28480 | 0160-0576 |
| A1C322 | 0160-0576 | 5 |  | CAPACITOR-FẊD . 1 UF +-20\% 50VDC CER | 28480 | 0160-0576 |
| A1C323 |  |  |  | NOT ASSIGNED |  |  |
| A1C324 | 0160-0576 | 5 |  | CAPACITOR-FXD . 1 UF +-20\% SOVDC CER | 28480 | 0160-0576 |
| A1C325 | 0180-3831 | 3 |  | CAPACITOR-FXD 10UF +-10\% 35VDC TA | 56289 | 2990106×9035081 |
| A1C326 |  |  |  | NOT ASSIGNEO |  |  |
| A1C327 | 0160-4040 | 6 |  | CAPACITOR-FXD 1000PF +-5\% 100VDC CER | 28480 | 0160-4040 |
| AtC328 | 0160-4040 | 6 |  | CAPACITOR-FXD 1000PF +-5\% 100VDC CER | 28480 | 0160-4040 |
| A1C329 AlC A | 0180-3775 | 4 |  | CAPACITOR-FXD 68UF +-20\% 10VOC TA | 28480 | 0180-3775 |
| A1C700 |  |  |  | NOT ASSIGNED |  |  |
| A1C70 1 | 0160-4787 |  | 2 | CAPACITOR-FXD 22-F +-5\% 100VDC CER O+-30 | 28480 | 0160-4787 |
| A1C702 | 0160-4787 | 8 |  | CAPACITOR-FXD 22-F +-5\% 100VDC CER 0+-30 | 28480 | 0160-4787 |
| A1C703 | 0180-3775 | 4 |  | CAPACITOR-FXD 68UF +-20\% 10VDC TA | 28480 | 0180-3775 |
| A1C704 | 0180-3775 | 4 |  | CAPACITOR-FXD 68UF +-20\% lovDC TA | 28480 | 0180-3775 |
| A1C705 | 0180-3775 | 4 |  | CAPACITOR-FXD 68UF +-20\% 10VDC TA | 28480 | 0180-3775 |
| A1C706 |  |  |  | NOT ASSIGNED |  |  |
| A1C70 7 | 0160-4557 | 0 |  | CAPACITOR-FXD . IUF +-20\% SOVDC CER | 16293 | CAC04K7R104M050A |
| A1C708 | 0160-4557 | 0 |  | CAPACITOR-FXD. IUF +-20\% SOVDC CER | 16299 | CAC04×7R104M050A |
| A1C709 | 0160-4557 | 0 |  | CAPACITOR-FXD . IUF +-20\% SOVDC CER | 16299 | CAC04X7R104M050A |
| A1C710 | 0160-4557 | 0 |  | CAPACITOR-FXD . 1 UF +-20\% 50VDC CER | 16299 | CAC04×7R104M050A |
| A1C711 | 0160-4557 | 0 |  | CAPACITOR-FXD. M | 16299 | CAC04K7R104M050A |
| A1C712 | 0160-4557 | 0 |  | CAPACITOR-FXD. 1 UF +-20\% SOVDC CER | 16299 | CAC04×7R104M1050A |
| A1C713 | 0160-4557 | 0 |  | CAPACITOR-FXD . IUF +-20\% SOVDC CER | 16299 | CAC04X7R1044050A |
| A1C714 | 0160-4557 | 0 |  | CAPACITOR-FXD. IUF *-20\% SOVDC CER | 16299 | CAC04×7R104M050A |
| AlC715 | 0160-4557 | 0 |  | CAPACITOR-FXD . IUF +-20\% SOVDC CER | 16299 | CAC04X7R104M050A |
| A1C716 | 0160-4557 | 0 |  | CAPACITOR-FXD. IUF *-20\% SOVOC CER | 16299 | CAC04×7R104M050A |
| A1C717 | 0160-4557 | 0 |  | CAPACITOR-FXD . 1UF +-20\% SOVDC CER | 16299 | CAC04×7R104M050A |
| A1C718 | 0160-4557 | 0 |  | CAPACITOR-FXD . IUF +-20\% SOVDC CER | 16299 | CAC04×7R104M050A |
| A1C719 | 0160-4557 | 0 |  | CAPACITOR-FXD . 1UF +-20\% SOVOC CER | 16299 | CACO 4×7R104M050A |
| A1c 720 | 0160-455? | 0 |  | CAPACITOR-FXD . IUF +-20\% SOVOC CER | 16299 | CAC04X7R104TIOSOA |
| AICR1 |  |  |  | NOT ASSIGNE.D |  |  |
| A1CR2 |  |  |  | NOT ASSIGNLD |  |  |
| A1CR3 | 1902-0939 | 9 | 3 | VOLTASE SUPPRESSOR VR $=5,0, \mathrm{VC}=8 \mathrm{~V}$ | 11961 | 1 1N5908 |
| A1CR4 | 1901-0050 | 3 | 26 | DIGOE-SWITCHING 8OV 200MA 2NS D0-35 | 9N171 | 1 N4150 |
| AICRS | 1901-0050 | 3 |  | OISOL-SHITCHING 8nV SOMA 2 NS 00-35 | 9N:71 | 1N4150 |
| A1CR6 | 1901-0050 | 3 |  | DTODE-SUITCHING 80 V 200MA 2 SS $00-35$ | 9N171 | 1 N 4150 |
| A1CR7 | 1901.0050 | 3 |  | GIODE-SUITCHING 80V 200MA 2NS D0-35 | 9N171 | 1 N 4150 |
| AICR8 | 1901-0050 | 3 |  | DIODE-SUITCHING 80 V 200MA 2 NS DO-35 | 9N171 | 1N4150 |
| AlCR9 | 1901-0050 | 3 |  | DIODE-SHITCHING 80V 200MA. 2NS D0-35 | 9N171 | 1 N 4150 |
| AlCR10 | 1901-0050 | 3 |  | DIODE-SHITHING 80V 200MA 2 NS DO-35 | 9N171 | 1N4150 |

See introduction to this section for ordering information *Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

| Reference Designation | HP Part Number | $\mathrm{C}$ | Qty | Description | Mir <br> Code | Mif Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A1CP1 | 1901-0050 | 3 |  |  | 9N171 | 1N4150 |
| A1CR12 | 1901-0050 | , |  | OIODE-SWITCHING 8DV 200MA 2 NS DO-35. | 9N171 | 1N4150 |
| A1CP13 |  |  |  |  |  |  |
| A1CP15 AlCP17 |  |  |  | NOT ASSIGNED OIODE-SWITCHING 80V 20GMA 2NS $00-35$ |  |  |
| A1CP17 | 1901-410, |  |  | [IUOE-SWITCHING 80V 20GMA 2NS [00-35 | GN171 | 1N4150 |
| A1cple: | 1901-00\% | 1 |  | DILOE -WITCHING 8OV 200mA 2 NS Dr is | 9N171 | 1N4150 |
| A1CR19 A1CR20 | 1901-037t |  | 4 | DIODE GEN PRP $35 V$ SOMA DO-35 NOT ASSIGNED | 9N17: | N3595 |
| A1CR21 | 1901-0050 | 3 |  | DIODE-SWITCHING 80V LOUMA DO-35 | 9N171 | 1N4150 |
| A1CR22 | 1901-0376 | 6 |  | DIODE-GEN PRP 35V SOMA DO. 35 | 9N171 | 1N3595 |
| A1CR23 | 1901-0518 | 8 | 2 | DIODE-SM SIG SCHOTTKY | 28480 | 1901-0518 |
| A1CR24 | 1901-0518 | 8 |  | OIODE SM SIG SCHOTTKY | 28480 | 1901-0518 |
| A1CR25 | 1901-0050 | 3 |  | OIODE-SUITCHING 80V 200mA 2NS DO- 35 | 9N171 | 1N4150 |
| A1CR2E | 1901-0050 | 3 |  | DIODE-SWITCHING 80V 200MA 2NS D0-35 | IN171 | 1N4150 |
| A1CR27 | 1901-0050 | 3 |  | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 9N171 | 1N4150 |
| A1CR28 | 1901-0376 | 6 |  | OIODE-GEN PRP 35V 50MA 00-35 | 9N171 | 1N3595 |
| A1CR29 | 1901-0376 | 6 |  | DIODE-GEN PRP 35V 50MA 00-35 | 9N171 | 1 N 3595 |
| A1CR30 | 1901-0050 | 3 |  | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 9N171 | - N4150 |
| A1CR31 | 1901-0050 | 3 |  | OIODE-SWITCHING 80V 200MA 2NS DO-35 | 9N171 | 1114150 |
| A1CR32 | 1901-0050 | 3 |  | OIODE-SWITCHING 80V TOOMA 2NS DO-35 | 9N171 | 1N4150 |
| A1CR33 | 1901-0050 | 3 |  | DIODE-SWITCHING SUV 200MA 2NS DO-35 | 9N171 | 1N4150 |
| A1CR34 | 1801-0050 | 3 |  | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 9N171 | 1N4150 |
| A1CR35 | 1901-0050 | 3 |  | DIODE-SWITCHING BOV 200MA 2NS D0-35 | 9N171 | 1N4150 |
| A1CR36 | 1901-0050 | 3 |  | OIODE-SWITCHING 80V 200MA 2NS DO-35 | 9N171 | 1N4150 |
| A1CR37 | 1902-0955 | 9 | , | OIODE - ZNR 7.5V 5\% 00-35-0..4W TC=0+.062\% | 28480 | 1902-0955 |
| A1CR38 | 1902-0956 | 0 | 2 | OIODE -ZNR 8.2V 5\% DO-35 PO=.4W TC=0 $+065 \%$ | 28480 | 1902-0956 |
| A1CR39 | 1902-0956 | 0 |  | DIODE -2NR 8.2V 5\% DO-35 PD=.4W TC=0+-065\% | 28480 | 1902-0956 |
| A1CR40 | 1902-0951 | 5 | 1 | DIODE-ZNR 5.1V 5\% DO-35 PD=.44 $\mathrm{IC}=+.035 \%$ | 28480 | 1902-0951 |
| $\begin{aligned} & \text { A1CR41- } \\ & \text { A1CR200 } \end{aligned}$ |  |  |  | NOT ASSIGNED |  |  |
| A12CR201 | 1906-0201 | 6 | 1 | OIODE-FU BRDG 400 V 4 A | 28480 | 1906-0201 |
| A 12 CR 202 | 1906-0096 | 7 | 1 | OIODE-FW BRDG 200V 2A | 04713 | MOA202 |
| $\begin{aligned} & \text { A12CR203 } \\ & \text { Al2CR204- } \end{aligned}$ | 1902-0939 | 9 |  | VOLTAGE SUPPRESSOR VR=5.0V VC=8V | 11961 | 1N5908 |
| A12CR290 |  |  |  | NOT ASSIGNED |  |  |
| AICR291 | 1901-0050 | 3 |  | DIODE-SUITCHING 80V 200mA 2NS D0-35 | 9N171 | 1N4150 |
| AlCR292 AlCR293- | 1901-0050 | 3 |  | DIODE-SUITCHING 80V 200MA 2NS DO-35 | 9N171 | 1N4150 |
| AlCR301 |  |  |  | NOT ASSIGNED |  |  |
| AlCR302 | 1900-0083 | 0 | 2 | DIODE-SCHOTTKY SM SIG | 28480 | 1900-0083 |
| AICR303 | 1900-0083 | 0 |  | DIODE-SCHOTTKY SM SIG | 28480 | 1900-0083 |
| A1CR304 | 1901-0050 | 3 |  | DIODE-SUITCHING 80V 200MA 2NS DO-35 | 9N171 | 1 N 4150 |
| A1CR305 <br> A1CR306- | 1901-0050 | 3 |  | DIODE-SUITCHING 80V 200MA 2NS DO-35 | 9N171 | 1 N 4150 |
| A1CP700 |  |  |  | NOT ASSIGNED |  |  |
| A1CR701 | 1902-0939 | 9 |  | VOLTAGE SUPPRESSOR VR=5.0V, VC $=8 \mathrm{~V}$ | 11961 | 1 N5908 |
| AlFi | 2110-0202 | 1 | 1 | FUSE . SA 250V TD 1.25x.25UL (FOR 100/120V OPERATION) | 75915 | 313.500 |
| AIF1 | 2110-0201 | 0 | 1 | FUSE .25A 250 V TD $1.25 \times .25 \mathrm{~L}$ (FOR 220/240V OPERATION) | $\begin{aligned} & 75915 \\ & 75915 \end{aligned}$ | $\begin{aligned} & 313.250 \\ & 313.250 \end{aligned}$ |
| A1JI | 1252-0268 | 8 | 1 | CONN-RECT MICRORBN 24-CKT 24-CONT | 28480 |  |
| A1J2 ${ }_{\text {AlJ }}$ | 1250-2109 | 6 | 4 | CONNECTOR-RF ENC FEM PCH-PNL 50-OHM | 24931 | 28JR405-1 |
| A1J10 |  |  |  | NOT ASSIGNED |  |  |
| AlJ 11 | 1250-2109 | $\varepsilon$ |  | CONNECTOR-RF CNE FEM PCH-PNL 50-OHM | 24931 | 28J4R05-1 |
| A1J12 | 1250-2109 | $\varepsilon$ |  | CONNECTOR-RF ENC FEM PCH-PNL 50-OHM | 24931 | 28JR405-1 |
| AlJ 13 | 1250-2109 | 6 | , | CONNECTOR-RF BNC FEM PCH-PNL 50-0HM | 24931 | 28JR405-1 |
| AlJ200 |  |  |  | NOT ASSIGNED |  |  |
| AlJ201 | 1252-0602 | 4 | 2 | CONN-UTIL P-\&-SKT 6-CKT 6-CONT | 23430 | 1252-0502 |
| AlJ202 | 1251-4743 | 0 | 1 | CONNECTIOR-aC PUR HP-9 Male pec-flt thrmp | 28480 | 1251-4743 |
| A 1 J 203 | 1252-0602 | 4 |  | CONN-UIIL P-\&-SKT 6-CKT E-CONT | 28480 | 1252-0602 |
| A1J 204 | 1252-3083 | 1 | 1 | CONNECIOP 2 -ROW $\times 15$-PIN RTANG | 28480 | 1252-3083 |
| AlJ 300 |  |  |  | NOT ASSIGNES |  |  |
| A 1 J301 | $1250-2109$ $1251-4504$ | 6 1 | 1 | CONNECTER RF-ENC PCMT FEM Pr.h-PNL 50-OHM | 03316 28480 | 28JR405-1 <br> 1251-4504 |
| A1J701 | 1251-4504 | 1 | 1 | CONN-POST TYPE . 100-PIN-SPCL 10 -CONT | 28480 | 1251-4504 |

See intraduction to this section for ordering information
*Indicates factory selected value
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Table 6-2. Replaceable Parts (Continued)

| Reference Designation | HP Part Number | $\begin{aligned} & C \\ & D \end{aligned}$ | Qty | Description | Mfr Code | Mif Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A1F1 | 0490-1317 | 3 | 4 | PELAY-REED ic 250ma 200VAC SVDC-COIL 3VA | 28480 | 04901-1317 |
| A1ki | 0490-1137 | 5 | 5 | RELAY-REED 1A 500MA 200VEC-COIL | 02744 | P.8868-1 |
| A1/3 | 0490-1317 | 3 |  | PELAY-REED IC 250ma 200VOC 5VDr-COIL 3Va | 28480 | $0490 \cdot 317$ |
| All 4 | 0490-1137 | 5 |  | PELAY-REED 1a 500ma zoovdc-coil | 02744 | F8868-1 |
| Alk | 0490-1317 | 3 |  | RELAY-REED IC 250Ma zoovoc svol. CoIL 3Va | 28480 | 0490-1317 |
| A) 16 | 0490-1137 | 5 |  | PFLAY-REEO 1a 500MA 200VOC-COIL | 02744 | R 8868 - 1 |
| Alk 7 | 0490-1137 | $\stackrel{5}{5}$ |  | FLAY-REED 1a 500ma 200VDC-COIL | 02744 | R8868-1 |
| Alk 8 | 0490-113 | 5 |  | relay-REED 1A 500MA 200VDC-COIL | 02744 | R8868-1 |
| Alt:9 | 0490-131, | 3 |  | RELAY-REED 1C 250ma 200 VDC SVDC-COIL 3 Va | 28480 | 0430-1317 |
| AlL1 | 9140-0536 | 4 | 2 | INDUCTOR RF-C.H-MLD 2UH 5\% . 105DX.26LG NOT ASSIGNED | 28480 | 9140-0536 |
| All 3 | 9170-0029 | 3 | 2 | CORE-SHIELOING BEAD | 28480 | 9170-0029 |
| A1L4 | 9170-0029 | 3 |  | CORE-SHIELDING BEAD | 28480 | 9170-0029 |
| $\begin{aligned} & \text { A1L5- } \\ & \text { A1L199 } \end{aligned}$ |  |  |  | NOT ASSIGNED |  |  |
| A1L200 | 9100-3060 | 1 | 2 | INDUCTOR 260UH 15\% | 28480 | 9100-3060 |
| All 201 | 9100-3060 | 1 |  | INOUCTOR 260UH 15\% | 28480 | 9100-3060 |
| A1L202 | 9140-0881 | 2 | 2 | INDUCTOR 4.7UH 10\% . 1970 -INX-433LG-IN | 28480 | 9140-0881 |
| Alleio | 9140-1170 | 4 | 1 | INOUCTOR 1.2UH $20 \%$.1980-INX.488LG-IN | 24228 | -18m121m-1 |
| A1L204 | 9140-0881 | 2 |  | INDUCTOR 4.7UH 10\% .1970-INX-433LG-IN | 28480 | 9140-0881 |
| $\begin{aligned} & \text { AlL205- } \\ & \text { All. } 209 \end{aligned}$ |  |  |  |  |  |  |
| AlL210 | 9140-0536 | 4 |  | INDUCTOR RF-CH-MLD 2 UH 5\% . 105DX. 26LG | 28480 | 9140-0536 |
| AiMP1 | 05334-00010 | 1 | 1 | ShiELD-RELAY | 28480 | 05334-00010 |
| A101 | 8153-0015 | 7 | 2 | TRANSISTOR PNP SI PD=200ME FT $=500 \mathrm{MHZ}$ | 28480 | 1853-0015 |
| A102 | -8153-001 ${ }^{\circ}$ | 7 |  | TRANSISTOR PNP SI PD $=200 \mathrm{ML}$ FT $=500 \mathrm{MHZ}$ | 28480 | $1853-0015$ |
| AlQ3 A104 | 1854-0246 | 8 | 1 | TRANSISTOR NPN SI TO-92 PD $=350 \mathrm{MU}$ NOT ASSIGNED | 04713 | SPS 233 |
| AlQS | 1854-0686 | 0 | 2 | TRANSISTOR NPN SI TO-72 PD= $200 \mathrm{M} 2 \mathrm{FT}=4 \mathrm{GHZ}$ | 28480 | 1854-0686 |
| Al06 | 1854-0636 | 0 | 2 | TRANSISTOR NPN SI TO-92 PD=350MU | 28480 | 1854-0636 |
| A107 | 1854-0636 | 0 |  | TRANSISTOR NPN SI TO-92 PD=350ML | 28480 | 1854-0636 |
| A108 | 1855-0327 | 8 | 2 | TRANSISTOR J-FET 2 N4416 N -CHAN D-MODE | 01295 | 2N4416 |
| A109 | 1855-0327 | 8 |  | TRANSISTOR J-FET 2 N4416 N -CHAN D-MODE | 01295 | 2N4416 |
| AlQ10 | 1854-0686 | 0 |  | TRANSISTOR NPN SI TO-72 PD=200M2 FT $=4 \mathrm{GHZ}$ | 28480 | 1854-0686 |
| A1R1 |  |  |  | NOT ASSIGNED |  |  |
| A1R2 AlR3 | 0757-0280 | 3 | 22 | RESISTOR $1 \mathrm{~K} 1 \%$. 1254 F TC=0 $=100$ NOT ASSIGNED | 24546 | CT4-1/8-T0-1001-F |
| A1R4 |  |  |  | NOT ASSIGNED |  |  |
| AIRS | 1810-0136 | 3 | 2 | NETWORK-RES 10-SIP MULTI-VALUE | 28480 | 1810-0136 |
| A1R6 | 1810-0136 | 3 |  | NETWORK-RES 10-SIP MULTI-VALUE | 28480 | 1810-0136 |
| A1R7 AlR8 | 0757-0397 | 3 | 1 | RESISTOR 68.1 i\% . 125w F TC= $=0+100$ NOT ASSIGNED | 24546 | CT4-1/8-T0-68R1-F |
| AlR9 | 1810-0405 | 9 | 1 | NETUORK-RES 8 -SIP 470.0 OHM $\times 4$ | 11236 | 750-83-R470 |
| AlR10 | 1810-0374 | 1 | 2 | NETWORK RES 8-SIP 1.OK OHM $\times 4$ | 11236 | 750-83-R1K |
| A1R11 | 1810-0374 | 1 |  | NETWORK RES 8-SIP 1.OK OHM $\times 4$ | 11236 | 750-83-R1K |
| A1R12 | 1810-0219 | 3 | 2 | NETWORK-RES 8-SIP 220.0 OHM $\times 4$ | 11236 | 750-83-R220 |
| A1R13 | 0757-0280 | 3 |  | RESISIOR 1K 1\%.125 ${ }^{\text {F }}$ F TC= $0+-100$ | 24546 | CT4-1/8-T0-1001-F |
| AlR14 | 0757-0394 | 0 | 6 | RESISIOR 51.1 $1 \% .125 \mathrm{~W}$ F TC= $0+-100$ | 24546 | CT4-1/8-T0-51R1-F |
| A1R15 | 0638-3442 | 9 | 2 | RESISTOR 237 1\% .125W F TC=0+-100 | 24546 | CT4-1/8-T0-237R-F |
| A1R16 |  |  |  | NOT ASSIGNED |  |  |
| A1R17 | 0698-3440 | 7 | 3 | RESISTOP 196 1\% . 125 W F TC $=0+-100$ | 24546 | CT4-1/8-T0-196R-F |
| A1R18 | 0698-3440 | 7 |  | RESISTOR 196 1\% .125W F TC $=0+-100$ | 24546 | CT4-1/8-T0-196R-F |
| A1R19 |  |  |  | NOT ASSIGNED |  |  |
| AlR20 | 0757-0280 | 3 |  | RESISTOR 1K 1\% . 125 W F $\mathrm{TC}=0+-100$ | 24546 | CT4-1/8-T0-1001-F |
| $\mathrm{A}_{1} \mathrm{P}_{21} 1$ | 0698-3156 | 2 | 1 | RESISTOR 14.7K 1\% . 125 W F TC=0 $+\cdots 100$ | 24546 | CT4-1/8-T0-1472-F |
| A1R22 A1R23 | 0698-0083 | 8 | 7 | RESISTOR 1.96 K 1\% . 125 W F $\mathrm{T}=0+-100$ NOT ASSIGNED | 24546 | CT4-1/8-T0-1961-F |
| A1P24 |  |  |  | NOT ASSIGNED |  |  |
| A1R25 | 0757-0442 | 9 |  | RESISTOR 10K 1\%.125W F TC $=0+-100$ | 24546 | CT4-1/8-T0-1002-F |
| $\begin{aligned} & \text { A1R26 } \\ & \text { A1R27 } \end{aligned}$ | 0698-3440 | 7 |  | RESISTOR 196 1\% . 125 w F $T C=0+100$ NOT ASSIGNED | 24546 | CT4-1/8-T0-196R-F |
| A1PC8 AlRes A)F 30 | 0757-0290 | 5 | 4 | RESISTOR $6.19 \mathrm{~K} \quad 1 \% \quad .125 \mathrm{~d}$ F $\mathrm{TC}=0+100$ <br> NOT ASSIGNED <br> NOI ASSIGNED | 19701 | 5033R-1/8-T0-6191-F |

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)


| Reference Designation | HP Part Number | $\begin{aligned} & C \\ & D \end{aligned}$ | Qty | Description | Mir Code | Mir Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A1P31 | 0698-3431 | 6 | 1 | FESISTOR 23.7 1\% . 125 w F TC $=0+100$ | 03888 | PME55-1/8-T0-23P7-F |
| A1P32 | 0757-0401 | 0 | 4 | PESISTOR 100 1\% . 125 W F TC $=0+-100$ | 24546 | C14-1/8-10-101-F |
| A1P33 | 0698-3443 | 0 | 4 | PESISTGP 287 1\% . 125 W F TC $=0+-100$ | 24546 | CT4-1/8-10-287P-F |
| A1R34 | 0898-0082 | 7 | 4 | PESISTOR $4641 \% .125 \mathrm{~W}$ F TC=0 +-100 | 24546 | CT4-1/8-10-4640-F |
| A1P35 | 0757-0280 | 3 |  | PESISTOP 1K 1\% . 125 W F IC $=0+100$ | 24546 | CT4-1/8-TC-1001-F |
| AIP36 | 1810-0292 | 2 | 1 | NETWORK-RES 14-DIP $\quad 00$ OHM $\times 1$ | 01121 | $31482^{\text {m }}$ |
| A1R37 | 1810-0364 | 9 |  | NETWORT-RES 6-SIP 4, 0 OHM $\times 5$ | 11236 | 750 6. R470 |
| A1R38 | 0757-1094 | 9 | 2 | RESIS 'UR $1.47 \mathrm{~K} 1 \% .125 \mathrm{w}$ F TC=0 +-100 | 24546 | CT4-1/8-10-1471-F |
| A1R39 | 0698-3150 | 6 | 2 | RESISTOP 2.37K 1\% . 125 W F TC $=0+-100$ | 24546 | CT4-1/8-T0-2371-F |
| A1P40 | 0757-0346 | 2 | 3 | RESISTOR 10 1\% . 125 F TC=0+-100 | 28480 | 0757-0346 |
| A1R41 | 2100-0558 | 9 | 3 | RESISTOR-TRMP 20k 10\% C TOP-AD' • TRN | 28480 | 2100-0558 |
| A1R42 | 0757-0416 | 7 | 4 | RESISTOR 511 1\% . 125 W F TC=0+10\% | 24546 | C14-1/8-T0-511P-F |
| A1 R43 | 0757-0416 | 7 |  | RESISTOR 511 1\%.125W F TC $=0+100$ | 24546 | C14-1/8-10-511R-F |
| AlR44 | 0757-0394 | 0 |  | RESISTOR 51.1 $1 \% .125 \mathrm{~W}$ F TC= $=0+100$ | 24546 | CT4-1/8-T0-51R1-F |
| A1R45 | 0698-0084 | 9 | 3 | RESISTOR 2.15K 1\% . 125 W F $\mathrm{TC}=0+100$ | 24546 | CT4-1/8-10-2151-F |
| A1R46 | 0757-0279 | 0 | 2 | RESISTOR 3.16K 1\% . 125 L F TC $=0+-100$ | 24546 | CT4-1/8-T0-3161-F |
| A1R47 | 0698-3446 | 3 | 1 | RESISTOR $383+-1 \% .125 \mathrm{~W}$ TF TC $=0+-100$ | 12482 | CT4-1/8-10-383R-F |
| AlRSO |  |  |  | NOT ASSIGNED |  |  |
| A1R51 | 0757-0401 | 0 | 4 | RESISTOR 100 1\% . 125 w F : $\mathrm{C}=0+100$ | 24546 | CT4-1/8-T0-101-F |
| AlR52 | 0698-3443 | 0 |  | RESISTOR 287 1\% .125 ${ }^{\text {F F T }}$ TC= $=0+-100$ | 24546 | CT4-1 8-10-287R-F |
| AIRS3 | 0757-0280 | 3 |  | RESISTOR 1K 1\%. 125 W F TC $=0+-100$ | 24546 | CT4-1/8-T0-1001-F |
| AlRS4 | 0698-0082 | 7 |  | RESISTOR 464 1\% .125w F TC $=0+-100$ | 24546 | CT4-1/8-10-4640-F |
| AlR55 | 0757-1094 | 9 |  | RESISTOR 1.47K $1 \%$. 125 W F TC $=0+100$ | 24546 | CI4-1/8-T0-1471-F |
| AlR56 | 0698-3150 | 6 |  | RESISTOR 2.37K 1\% . 125 L F $\mathrm{TC}=0+-100$ | 24546 | CT4-1/8-T0-2371-F |
| A1R57 | 0757-0346 | 2 |  | RESISTOR 10 1\%. 125 F TC=0+-100 | 28480 | 0757-0346 |
| A1R58 | 2100-0558 | 9 |  | RESISTOR-TRMR 20K 10\% C TOP-ADJ 1-TRN | 28480 | 2100-0558 |
| AlR59 | 0757-0394 | 0 |  | RESISTOR 51.1 1\%. 125 W F TC $=0+-100$ | 24546 | CT4-1/8-T0-51R1-F |
| AlR60 | 0698-3155 | 1 | 5 | RESISTOR 4.64K 1\% . 125 W F $\mathrm{TC}=0+-100$ | 24546 | CT4-1/8-T0-4641-F |
| AlR61 | 0698-0084 | 9 |  | RESISTOR 2.15K 1\% .125W F TC $=0+100$ | 24546 | CT4-1/8-T0-2151-F |
| A1R62 | 0698-3155 | 1 |  | RESISTOR 4.64K 1\% . 125 W F TC $=0+-100$ | 24546 | CT4-1/8-10-4641-F |
| A1R63 | 0698-3455 | 4 | 2 | RESISTOR 261K 1\%. 125 W F TC $=0+-100$ | 24546 | C14-1/8-T0-2613-F |
| A1R64 | 0688-8960 | 6 | 2 | RESISTOR 750K 1\%.125 W F TC $=0+-100$ | 28480 | 0698-8960 |
| A1R65 |  |  |  | NOT ASSIGNED |  |  |
| A1R66 |  |  |  | NOT ASSIGNED |  |  |
| A1R67 | 2100-3253 | 7 | 2 | RESISTOR-TRMR 50K $10 \%$ C TOP-ADJ 1-TRN | 28480 | 2100-3253 |
| A1R68 | 0698-8958 | 2 | 4 | RESISTAR S11K 1\% . 125w F TC $=0+-100$ | 28480 | 0698-8958 |
| AlR69 | 0698-0083 | 8 |  | RESISIOR 1.96K $1 \% .125 \mathrm{WF}$ TC $=0+-100$ | 24546 | CT4-1/8-T0-1961-F |
| A1R70 | 0698-0083 | 8 |  | RESISTOR 1.96K 1\% . 125 W F TC $=0+-100$ | 24546 | CT4-1/8-T0-1961-F |
| A1R71 | 0698-3154 | 0 | 2 | RESISIOR 4.22K 1\% . 125 WJ F TC $=0+100$ | 24546 | CT4-1/8-70-4221-F |
| A1R72 | 0698-3154 | 0 |  | RESISTOR 4.22K 1\%. 125 W F IC $=0+-100$ | 24546 | CT4-1/8-70-4221-F |
| A1R73* | 0757-0398 | 4 | 2 | RESISTUR 75 1\%. 125 L F TC $=0+-100$ | 24546 | CT4-1/8-T0-75R0-F |
| A1R74 | 0757-0438 | 3 | 1 | RESISTOR 5.11K 1\%.125w F TC= $0+-100$ | 24546 | CT4-1/8-T0-5111-F |
| A1R75 | 0757-0416 | 7 |  | RESISTOR 511 1\% .125w F TC= $0+-100$ | 24546 | CT4-1/8-T0-511R-F |
| A1R76 | 0757-0416 | 7 |  | RESISTOR $5111 \% .1256$ F TC $=0+-100$ | 24546 | CT4-1/8-T0-511R-F |
| A1R77 | 0757-0394 | 0 |  | RESISTOR 51.1 1\%.125w F TC $=0+-100$ | 24546 | CT4-1/8-T0-51R1-F |
| A1R78 | 0699-0073 | 8 | 2 | RESISTOR 101 M i\% . 12 S 4 L F TC $=0+-150$ | 28480 | 0699-0073 |
| A1R79 | 0757-0279 | 0 |  | RESISTOR 3.16K $1 \% .1256 \mathrm{~J}$ F TC $=0+100$ | 24546 | CT4-1/8-T0-3161-F |
| A1R80 | 0757-0394 | 0 |  | RESISTOR 51.1 1\%.125 F F TC $=0+-100$ | 24546 | CT4-1/8-T0-51R1-F |
| AlR81 | 0699-0073 | 8 |  | RESISTOR 10M 1\%.125 ${ }^{\text {F F TC }}=0+-150$ | 28480 | 0699-0073 |
| A1R82 | 0698-8958 | 2 |  | RESISTOR 511K $1 \% .125 \mathrm{~W}$ F TC $=0+-100$ | 28480 | 0698-8958 |
| A1R83 | 0698-3260 | 9 | 2 | RESISTOR 4G4K 1\%. 125 W F TC $=0+-100$ | 28480 | 0698-3260 |
| A1R84 | 0757-0440 | 7 | 2 | RESISTOP $7.5 K^{\prime} 1 \% .125 \mathrm{H}^{\text {F }}$ TC $=0+-100$ | 24546 | CT4-1/8-T0-7501-F |
| A1R85 | 2100-3253 | 7 |  | RESISTOR-TRMR 50K 10\% ¢ TOP-ADJ 1-TRN | 28480 | 2100-3253 |
| A1R86 | 0698-0083 | 8 |  | RESISTOR 1.96K 1\% . 125 W F TC $=0+-100$ | 24546 | CT4-1/8-T0-1961-F |
| A1R87 | 0698-0083 | 8 |  | RESISTOR 1.96k, 1\% . 125 L F TC $=0+-100$ | 24546 | CT4-1/8-T0-1961-F |
| AlR88 | 0698-0083 | 8 |  | RESISTOR 1.96k 1\% . 125 W F TC=0+-100 | 24546 | CT4-1/8-T0-1961-F |
| A1R89 |  |  |  | NOT ASSIGNED |  |  |
| A1R90* | 0757-0398 | 4 |  | RESISTUR 75 1\% . 125w F $1 \mathrm{C}=0+-100$ | 24546 | CT4-1/8-T0-75R0-F |
| A1R91 |  |  |  | NOT ASSIGNED |  |  |
| A1R92 |  |  |  | NOT ASSIGNED |  |  |
| A1R93 | 0757-0466 | 7 | 2 | RESISTOR 110k $1 \% .1254$ F TC $=0+-100$ | 24546 | CT4-1/8-T0-1103-F |
| A1R94 | 0698-3456 | 5 | 1 | RESISTOP 287k 1\% . 125 J F F IC $=0+-100$ | 24546 | CT4-1/8-T0-2873-F |
| A1R95 | 0698-3455 | 4 |  | RESISTOR 261K 1\% . 125 W F TC $=0+-100$ | 24.46 | CT4-1/8-T0-2613-F |

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

| Reference Designation | HP Part Number | $\mathrm{C}$ | Qty | Description | Mir Code | Mir Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A1R96 | 0698-8960 | $\xi$ |  | PESISTAP 750k. 1\% . 125 W F TS $=0+-100$ | 28480 | 0698-8960 |
| 41897 | 0698-3266 | 5. | 2 | PESISTOR 237k $1 \% .1256$ F TC $=0+100$ | 2454E | CT4-1/8-T0-2373-F |
| A1R98 | 0757-046\% | 7 |  | RESISTOR 110k 1\% . 125 W F F TC $=0+-100$ | 2454E | CT4-1/8-T0-1103-F |
| A1R99 | 0757-0178 | 8 | 4 | RESISTOP 100 1\% . 25w F TC $=0+-100$ | 24548: | NAS-1/4-T0-101-F |
| AlP100 | 0757-0178 | 8 |  | RESISTOR 100 1\% . 25 W F TC=0. 190 | 2454E | NAS-1/4-TC $101-F$ |
| Alfici | 069\% 3443 | ${ }_{0}$ | 4 | RESISIOP 287 1\% . 125W F Tr. $=0+-100$ | 24546 | TT4-1/8-T0-287R-F |
| AlFio2 | 2100-3252 | $\varepsilon$ | 2 | RESISTOR-TPMR 5K 10\% C TOP-ADJ 1-TRN | 28480 | 2100-3252 |
| AIPIO? | 2100-3252 | $\varepsilon$. |  | RESISTOR-TRMP 5K 10\% C TOP-ADJ 1-TRN | 28480 | 2100-3252 |
| AIR104 | 0698-8958. | 2 |  | RESISTOR $511 \mathrm{~K} 1 \% .125 \mathrm{~W}$ F TC $=0+-100$ | 28480 | 0638-8958 |
| Alplos | 0698-0083 | 8 |  | RESISTOR $1.96 \mathrm{~K} \quad 1 \% .125 \mathrm{WF}$ TC $=0+-100$ | 24546 | CT4-1/8-T0-1961-F |
| A1R106 | 0757.0290 | 5 |  | RESISTOR 6.19K 1\% . 125 LJ F TC $=0+-100$ | 19701 | 5033R-1/8-10-6191-F |
| A1R107 | 0757-0290 | 5 |  | RESISTOR 6.19K 1\% . 125 W F TC $=0+100$ | 19701 | 5033R-1/8-T0-6191-F |
| AIP108 | 0698-3432 | 7 | 3 | RESISTOR 26.1 1\% . 125 L F TC $=0+-100$ | 03888 | PME55-1/8-T0-26R1-F |
| A1R109 | 0698-3266 | 5 |  | RESISTOR 237K 1\% . 1250 FF TC $=0+-100$ | 24546 | CT4-1/8-T0-2373-F |
| AIRI10 | 0698-8958 | 2 |  | RESISTOR 511K 1\% . 125 w F TC=0+-100 | 28480 | 0698-8958 |
| A1R111 | 0698-3260 | 9 |  | RESISTOR 464K 1\% . 125 W F TC $=0+-100$ | 28480 | 0698-3260 |
| A1R112 | 0757-0440 | 7 |  | RESISTOR 7.5K 1\%.125U F TC $=0+-100$ | 24546 | CT4-1/8-T0-7501-F |
| A1R113 | 0698-3432 | 7 |  | RESISTOR 26.1 1\% . 125 W F TC=0+-100 | 03888 | PMES5-1/8-TO-26R1-F |
| AlR114 AlR115 |  |  |  | NOT ASSIGNED <br> NOT ASSIGNED |  |  |
| AlR116 | 0698-8961 | 7 | : | RFSISTOR 909K 1\% . 125 L F TC $=0+-100$ | 2¢ 180 | 0698-8961 |
| AlR117 | 0698-8961 | 7 |  | RESISTOR 909K 1\% . 125 L F TC $=0+-100$ | 28480 | 0698-8961 |
| A1R118 | 1810-0219 | 3 |  | NETWORK-RES 8 -SIP 220.0 OHM $\times 4$ | 11236 | 750-83-R220 |
| A1R119 | 1810-0347 | 8 | 1 | NETWORK-RES 8-SIP 2.2F OHM $\times 4$ | 11236 | $750-80-R 2.2 K$ |
| AIR120 | 0757-0178 | 8 |  | RESISTOR 100 \% . 25 W F TC $=0+-100$ | 24546 | NAS-1/4-10-101-F |
| A1R121 | 0757-0178 | 8 |  | RESISTOR $1001 \% .25 \mathrm{~W}$ F TC $=0+-100$ | 24546 | NA5-1/4-T0-101-F |
| $\begin{aligned} & \text { A1R122 } \\ & \text { A1R123- } \end{aligned}$ | 0757-0418 | 9 | 1 | RESISIOR 619 1\% . 1256 F IC $=0+-100$ | 24546 | CT4-1/8-10-619R-F |
| A1R125 |  |  |  | NOT ASSIGNED |  |  |
| A1R126 | 1810-0280 | 8 | 5 | NEILUORK-RES 10 -SIP 10.0 K OHM $\times 9$ | 91637 | CSC10A01-103G/M5P10A01- |
| A1R127 | 0757-0442 | 9 |  | RESISTOR 10K 1\% . 125 W F TC=0+-100 | 24546 | CT4-1/8-10-1002-F |
| A1R128 | 0757-0280 | 3 |  | RESISIOR 1K 1\% . 125 LJ F TC $=0+100$ | 24546 | CT4-1/8-T0-1001-F |
| A1R129 | 0757-0280 | 3 |  | RESISTOR $1 \mathrm{~K} 1 \% .125 \mathrm{LJ}$ F TC=0 $0-100$ | 24546 | CT4-1/8-T0-1001-F |
| A1R130 | 2100-2216 | 0 | 2 | RESISTOR-TRMR 5K 10\% C TOP-ADJ 1-TFN | 73138 | 82PR5K |
| A1R131 | 2100-2216 | 0 |  | RESISTOR-TRMR 5K 10\% C TOP-ADJ 1-TRN | 73138 | 82PR5K |
| A1R132 | 2100-2060 | 2 | 2 | RESISTOR-TRMR 50 20\% C TOP-ADJ 1 - TKN | 73138 | 82PR50 |
| A1R133 | 2100-2060 | 2 |  | RESISTOR-TRMR 50 20\% C TOP-ADJ 1-TRN | 73138 | 82PR50 |
| A1R134 | 0757-0394 | 0 |  | RESISTOR 51.1 1\% . 125 LJ F TC $=0+100$ | 24546 | CT4-1/8-T0-51R1-F |
| A1R135 | 1810-0203 |  | 1 | NETWORK RES 8-SIP 470.0 OHM $\times 7$ | 28480 | 1810-0203 |
| $\begin{aligned} & \text { A1R136- } \\ & \text { A1R139 } \end{aligned}$ |  |  |  | NOT ASSIGNED |  |  |
| A1R140 | 1810-0367 | 2 | 1 | NETWORK-RES 6-SIP 4.7K OHM $\times 5$ | 11236 | 750-61-R4.7K |
| AlR141 | 1810-0280 | 8 |  | NETWORK-RES 10-SIP 10.0K OHM $\times 9$ | 91637 | CSC10A01-A03G/MSP10A01- |
| A1R142 | 0698-0082 | 7 |  | RESISTOR 464 1\% . 125 W F TC $=0+-100$ | 24546 | CT4-1/8-10-4640-F |
| A1R143 | 2100-4158 | 3 | 1 | RESISTOR-TRMR 10K 10\% TKF TOP-ADJ 25-TRN | 28480 | 2100-4158 |
| A1R144 A1R145- | 0757-0290 | 5 |  | RESISTOR 6.19K 1\% . 125 W F TC $=0+-100$ | 19701 | 5033R-1/8-10-6191-F |
| A1R200 |  |  |  | NOT ASSIGNED |  |  |
| A1R201 | 0698-3443 | 0 |  | RESISTOR 287 1\%. 125U F TC=0 +-100 | 24546 | CT4-1/8-T0-287R-F |
| AlR202 | 2100-0568 | 1 | 1 | RESISTOR-TRMR 100 10\% C TOP-ADJ 1-TRN | 28480 | 2100-0568 |
| A1R203 | 0698-3442 | 9 |  | RESISTOR 237 1\% .125 ${ }^{\text {F }}$ FTC $=0+-100$ | 24546 | CT4-1/8-10-237R-F |
| A1R204- A1R209 |  |  |  | NOT ASSIGNED |  |  |
| AlR210 | 0757-0280 | 3 |  | RESISTOR IK ix . 125 W F TC $=0+100$ | 24546 | CT4-1/8-T0-1001-F |
| AlR211 | 0698-3432 | 7 |  | RESISTOR 26.1 i\% . 125 w F $\mathrm{TC}=0+100$ | 03888 | PME55-1/8-T0-26R1-F |
| $\begin{aligned} & \text { A1R212- } \\ & \text { AlR260 } \end{aligned}$ |  |  |  | NOT ASSIGNED |  |  |
| AlR261 | 0757-0280 | 3 |  | RESISTOR 1K 1\% . 125 W F TC $=0+100$ | 24546 | CT4-1/8-T0-1001-F |
| AlR262 | 0757-0280 | 3 |  | RESISTOR 1K 1\%. 125 W F TC $=0+100$ | 24546 | CT4-1/8-T0-1001-F |
| AlR263 | 0757-0280 | 3 |  | RESISTIAR IK 1\% . 125 L W F TC $=0+100$ | 24546 | CT4-1/8-T0-1001-F |
| AlR264 | 0757-0280 | 3 |  | RESISTOR 1K 1\% . 125 W F $\mathrm{TC}=0+100$ | 24546 | CT4-1/8-T0-1001-F |
| AlR265 | 0757-0280 | 3 |  | PESISTOR 1K 1\% .125 F F TC=0+-100 | 24546 | CT4-1/8-T0-1001-F |
| A1R266- |  |  |  | NOT ASSIGNED |  |  |
| A1R270 |  |  |  | NOT ASSIGNED |  |  |
| A1R271 | 8159-0005 | 0 | 19 | RESISTOR-ZERO OHMS 22 allg lead oia | 2480 | 8159-0005 |
| A1R272 | 8159-0005 | 0 |  | RESISTOR-ZERO OHMS 22 Aldg lead oia | 2480 | 8159-0005 |
| AlR273 | 8159-0005 | 0 |  | RESISTOP ZEPO OHMS 22 allg lean dia | 2480 | 8159-0005 |
| AlR274 | 8159-0005 | 0 |  | RESISTOR-2ERO OHMS 22 AUG LEAEI DIA | 2480 | 8159-0005 |
| A1R275 | 8159-0005 | 0 |  | RESISTOR-ZERO OHITS 22 Aldg lean dia | 2480 | 8159-0005 |

See introduction to this section for ordering information ${ }^{*}$ Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)


Table 6-2. Replaceable Parts (Continued)

| Reference Designation | HP Part Number | $\begin{aligned} & C \\ & D \end{aligned}$ | Qty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { A1P718- } \\ & \text { A1P7E0 } \end{aligned}$ |  |  |  | NOT ASSIGNED |  |  |
| A1P761 | 0757-0280 | 3 |  | PESISTOR ik 1\% . 125 ${ }^{\text {d }}$ F TC $=0+-100$ | 24546 | C74-1/8-10-1001-F |
| A1P762 | 0757-028 | 3 |  | RESISTOR 1K 1\%.125 F F TC $=0+-10 \mathrm{C}$ | 24546. | CT4-1/8-10-1001-F |
| AlP763 | 0757-028! | 3 |  | RESISTOR 1K $1 \% .125 \mathrm{~d}$ F TC $=0+100$ | <4546 | CT4-1/8-10-1001-F |
| A1P764 | 0757-0280 | $\Sigma$ |  | PESISTIP $1 \mathrm{~K} 1 \% .125 \mathrm{U}$ F TC $=0+100$ | 24546 | CT4-1/8-10-1001-F |
| Alp765 | 0757-0280 | 3 |  | RESISTOR 1K 1\% . 125 LJFT TC=0+-100 | 24546 | CT4-1/8-10-1001-F |
| AlS 1 | 3101-2567 | 7 | 1 | SUItCh IGL SUBMIN DPUT -A İOVAC PC | 28480 | 3101-2567 |
| $\begin{aligned} & \text { A1S2 } \\ & \text { A153- } \end{aligned}$ | 3101-2457 | 4 | 1 | SWITCH-P8 4PDT ALTNG 4A 250VAC | 28480 | 3101-2457 |
| A1 S200 |  |  |  | NOT ASSIGNED |  |  |
| A15201 | 3101-2340 | 4 | 1 | SUITCH-RKR OIP-RKR ASSY 5-1A .O5A 3OVDC | 28480 | 3101-2340 |
| A1S202 | 3101-2693 | 0 | 2 | SUITICH-SL DPDI STD 5A 250VAC PC | 28480 | 3101-2693 |
| A15203 | 3101-2693 | 0 |  | SUITCH-SL DPOT STD 5a 250VAC PC | 28480 | 3101-2693 |
| A1SP1 | 1258-0141 | 8 | 1 | JUMPER-REMOVABLE FOR 0.025 IN SQ PINS | 28480 | 1258-0141 |
| A1TP1 | 0360-0124 | 3 | 21 | CONNECTOR-SGL CONT PIN . 04 -IN-BSC-SZ | 28480 | 0360-0124 |
| A1TP2 | 0360-0124 | 3 |  | CONNECTUR-SGL CONT PIN 04 -IN-BSC-S2 | 28480 | 0360-0124 |
| AltP3 | 0360-0124 | 3 |  | CONHECTOR-SGL CONT PIN . 04 - IN-BSC-SZ | 28480 | 0360-0124 |
| A1TP4 | 0360-0124 | 3 |  | CONNECTOR-SGL CONT PIN . 04 - IN-BSC-SZ | 28480 | 0360-0124 |
| AlTPS | 0360-0124 | 3 |  | CONNECTOR-SGL CONT PIN . 04 -IN-BSC-SZ | 28480 | 0360-0124 |
| A1TP6 | 0360-0124 | 3 |  | CONNECTOR-SGL CONT PIN . $04-$ IN-BSC-SZ | 28480 | 0360-0124 |
| A1TP7 | 0360-0124 | 3 |  | CONNECTOR-SGL CONT PIN . 04 -IN-BSC-S2 | 28480 | 0360-0124 |
| A1TP8 | 0360-0124 | 3 |  | CONNECTOR-SGL CONT PIN . 04 -IN-BSC-SZ | 28480 | 0360-0124 |
| A1TP9 | 0360-0124 | 3 |  | CONNECTOR-SGL CONT PIN . 04 -IN-BSC-SZ | 28480 | 0360-0124 |
| A1TP10 | 0360-0124 | 3 |  | CONNECTOR-SGL CONT PIN . $04-\mathrm{IN}$-BSC-SZ | 28480 | 0360-0124 |
| AltP1 1 | 0360-0124 | 3 |  | CONNECTOR-SGL CONT PIN . 04 -IN-BSC-SZ | 28480 | 0360-0124 |
| A1TP12 | 0360-0124 | 3 |  | CONNECTOR-SGL CONT PIN . 04 -IN-BSC-SZ | 28480 | 0360-0124 |
| Altpl3 | 0360-0124 | 3 |  | CONNECTOR-SGL CONT PIN . 04 -IN-BSC-SZ | 28480 | 0360-0124 |
| AlTP14 | 0360-0124 | 3 |  | CONNECTOR-SGL CONT PIN . 04 -IN-BSC-SZ | 28480 | 0360-0124 |
| A1TP15 | 0360-0124 | 3 |  | CONNECTOR-SGL CONT PIN . 04 -IN-BSC-SZ | 28480 | 0360-0124 |
| A1TP16 | 0360-0124 |  |  | CONNECTOR-SGL CONT PIN . 04 -IN-BSC-SZ | 28480 | 0360-0124 |
| A1TP17 | 0360-0124 | 3 |  | CONNECTOR-SGL CONT PIN . 04 -IN-BSC-SZ | 28480 | 0360-0124 |
| AlTP18 | 0360-0124 | 3 |  | CONNECTOR-SGL CONT PIN . 04 -IN-BSC-SZ | 28480 | 0360-0124 |
| A1TP19 | 0360-0124 | 3 |  | CONNECTOR-SGL CONT PIN . 04 -IN-BSC-SZ | 28480 | 0360-0124 |
| A1TP20 | 0360-0124 | 3 |  | CONNECTOR-SGL CONT PIN . 04 -IN-BSC-SZ | 28480 | 0360-0124 |
| AlTP21 | 0360-0124 | 3 |  | CONNECTOR-SGL CONT PIN . 04 -IN-BSC-SZ | 28480 | 0360-0124 |
| AItT1 | 0340-0090 | 0 | 2 | INSULATOR-BDG POST PLASTIC | 28480 | 0340-0090 |
| Altte | 0340-0090 | 0 |  | INSULATOR-GDG POST PLASTIC | 28480 | 0340-0090 |
| Alus |  |  |  | NOT ASSIGNED |  |  |
| Alu6 | 1820-3121 | 3 | 1 | IC TTL 74ALS $245 \times \mathrm{XC4}$ | 01698 | SN74ALS245AN |
| AlU7 | 1820-2058 | 3 | 1 | IC TRANSCEIVER TTL S INSTR-BUS-IEEE-488 | 04713 | MC3448AL |
| Alu8 | 1820-1425 | 6 | 1 | IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP | 01295 | SN74LS132N |
| Alug | 1820-3270 | 3 | 1 | IC GATE TTL TTL/ALS NAND QUAD 2-INP | 01698 | SN74ALSO3BN |
| Alvio | 1820-3479 | 4 | 1 | IC DRVR TTL ALS NOR QUAD 2 -INP | 01295 | SN74ALS28AN |
| Aluli | 1820-0810 | 1 | 1 | IC RCVR ECL LINE RCVR TPL 2-INP | 04713 | MC10116P |
| Aluiz | 1820-2096 | 9 | 2 | IC CNTR TTL LS 日in dual 4-bit | 01295 | SN74L5393n |
| Alui3 | 1820-2096 | 9 | 2 | IC CNTR TTL LS BIN dual 4-bit | 01295 | SN74LS393N |
| Alul 4 | 1820-2709 | 1 | 1 | IC MISS ECL | 28480 | 10A7C8R |
| AlU15 | 1820-3438 | 5 | 2 | Ii muxr/gata-sel til als 2-to-1 LINE | 01295 | SN74ALS257N |
| Alut6 | 1820-3438 | 5 |  | If MUXR/DATA-SEL ITL ALS 2-TO-1 LINE | 01295 | SN74ALS257N |
| Alvil | 1820-5349 | 1 | 1 | MCU 38P74 4K ROM | 28480 | 1820-5349 |
| A1U17A | 1820-2650 |  | 1 | IC, NMOS MCU | 28480 | 1820-2650 |
| Alllis | 1813-0150 | 7 | 1 | If OSC CMOS | 32293 | ICM7209IPA |
| Alu19 | 1820-5347 | 9 | 1 | MCU 38P78 8K ROM | 28480 | 1820-5347 |
| Alu20 | 1820-2312 | 2 | 1 | IC MISC | 28480 | 10A9-2902 |
| Alu21 | 1820-3125 | 7 | 1 | IC XLTR ECL ECL-TO-TtL QUAD | 02037 | MC10125P |
| Alu22 | 1825-0426 | 7 | 1 | IC COMPARATOR HS DUAL 16-DIP-C PKG | 34335 | AM687ADL |
| Alu23 | 1826-0493 | 8 | 2 | IC OP AITP LOU-BIAS-H-IMPD 8-DIP-P PkG | 04713 | MLM308AP1 |
| Alu24 | 1820-1053 | 6 | 1 | IC. SCHMITT-TRIG TTL INV HEX | 01295 | SN7414N |
| AlU25 | 1926-0315 | 3 | 1 | IC OP AMP GP OUACI 14-DIP-P PKG | 27014 | LM348N |
| A1U26 | 1820-3692 | 3 | 3 | IC. ANLG-IIUXR/DEMUXR CMOS/74HC 2-CHANNEL | 27014 | MM74HC4053N |
| Alu27 | 1820-3692 | 3 |  | IC. ANLG-MIIXR/DEMUIXR CMOS/74HC 2-CHANNEL | 27014 | MM74HC.4053N |
| Alu28 | 1820-3692 | 3 |  | IC ANLG-MUXR/DEMUXR CMOS/74HC 2-CHANNEL | 27014 | MM74HC 4053N |
| A1u29 | 1820-5348 | 0 | 1 | MCU SSP74 4K ROM | 28480 | 1820-5348 |
| Alu30 | 1826-0493 | 8 |  | If OP AIP LOw-bIAS H-IMPD 8-DIP-P PKG | 04713 | MLM308AP1 |

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)

| Reference Designation | HP Part Number | $\left\lvert\, \begin{aligned} & C \\ & D \end{aligned}\right.$ | Qty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A1U31 | 1820-3145 | 1 | 1 | If DRVP TTL ALS BUS OCTL | 01295 | SN74LS244AN |
| A1U32 | 1820-1827 | 2 | , | IC DCDR CMOS 4-TO-16-LINE | 27014 | M1174C 154N |
| Alu33 | 1826-0639 | 4 | 2 | 0/A 8-BIT 16-PLASTIC CMOS | 24355 | A07524JN |
| Alu34 | 1826-0639 | 4 |  | D/A 8-BIT 16-PLASTIC CMOS | 24355 | A07524JN |
| Alu35 | 1826-0544 | 0 | 1 | IC V PGLTR V-REF FXD 2.5 V 8POIP-C PKG | 28480 | 1826-0544 |
| Alu36 | 1826-0412 | 1 | 3 | IC COMPARATOR PRCN DUAL 8-DIP-P PKG | 27014 | LM393N |
| AlU37 | 1820-1997 | 7 | 1 | IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN | 34335 | AM74LS374AP |
| Alu38 | 1820-0471 | 0 | 1 | IC INV TTL HEX 1-INP | 01295 | SN7406N |
| AlU39 | 1820-4458 | 1 | 1 | IC BFR CMOS-74HC BUS QUAD | 04713 | MC74HC126N |
| Alu Alu20 |  |  |  | NOT ASSIGNED |  |  |
| Aluz01 | 1826-1597 | 5 | 3 | IC V RGLTR-FXD-POS 4.85/5.15V T0-220 PKG | 27014 | LM2940CT-5.0 |
| A1U202 | 1826-1597 | 5 | 3 | IC $V$ RGLTR-FXD-POS 4.85/5.15V TO-220 PKG | 27014 | LM2940CT-5.0 |
| Aluz03 | 1826-0393 | 7 | 1 | IC $V$ RGLTR-ADJ-POS $1.2 / 37 \mathrm{~V}$ T0-220 PKG | 8280 | 1826-0393 |
| Alu204 | 1826-0215 | 2 | 1 | IC $V$ RGLTR-FXD-NEG 5/5.4V T0-220 PKG | 04713 | MC7905.2CT |
| A1U205 | 1826-0147 | 9 | 1 | IC $7812 \vee$ RGLTR TO-220 | 04713 | MC7812CP |
| $\begin{aligned} & \text { A1U206- } \\ & \text { A1U290 } \end{aligned}$ |  |  |  | NOT ASSIGNED |  |  |
| A1U291 | 1826-0412 | 1 |  | IC COMPARATOR PRCN DUAL 8-DIP-P PKG | 27014 |  |
| A1u292 | 1826-1338 | 2 | 1 | IC MISC 8-DIP-P PKG | 01717 | TL.7705A |
| AlU293. A1U300 |  |  |  | NOT ASSIGNED |  |  |
| Alu301 | 1820-2848 | 9 | 1 | IC RCVR ECL/10KH LINE RCVR TPL104713 | 04713 | MC10H116P |
| A1U302 | 1820-5276 | 3 | 1 | IC-PRESCR ECL | 06344 | ME506. DIP- 8 |
| Alu303 | 1826-1614 | 7 | 3 | IC RF/IC AMPL 4-CuStom Pkg | 04713 | MUA0204 |
| A1U304 | 1826-1614 | 7 | 3 | IC RF/IC AMPL 4-CUSTOM PKG | 04713 | MUA0204 |
| A1 U305 | 1826-1614 | 7 |  | IC RF/IC AMPL 4 -CUSTOM PKG | 04713 | MWA0204 |
| A1U306 | 1826-0412 | 1 |  | IC COMPARATOR PRCN DUAL 8-dip-p PKg. | 27014 | LM393N |
| $\begin{aligned} & \text { A1U307- } \\ & \text { A1U700 } \end{aligned}$ |  |  |  | NOT ASSIGNED |  |  |
| Alu701 | 1826-1597 | 5 |  | IC $V$ RGLTR-FXD POS 4.85/5.15V T0-220-PKG | 27014 | LM2940CT-5.0 |
| A10702 | 1820-3157 | 5 | 1 | IC MPU; CLK FREQ $=1 \mathrm{MHZ}$; HERMETIC ; $1 / 0 ; 8$-GITS | 8280 | 1820-3157 |
| Alu703 | 1820-2724 | 0 | 5 | IC LCH TTL ALS TRANSPARENT OCTL. | 01295 | SN74ALS573BN |
| Alu704 | 1820-3121 | 3 | 1 | IC TRANSCEIVER TTL ALS bus octl | 01295 | SN74ALS245AN |
| A14705 | 1820-2724 | 0 |  | IC LCH TIL ALS TRANSPARENT OCTL | 01295 | SN74ALS5738N |
| Alu706 | 1820-2724 | 0 |  | IC LCH TTL ALS TRanSParent octi | 01295 | SNT4ALSS538N |
| A14707 | 1820-2634 | , | 2 | IC INV TTL ALS HEX | 01295 | SN74ALSO4EN |
| Alu708 | 1818-3183 | 2 | 1 | IC CMOS 65536 (64K) STAT RAM $150-\mathrm{NS} 3-5$ | S4013 | HH6264LP-15 |
| AlU709 | 1818-3465 | 3 | 1 | IC NMOS 262144 (256K) EPROM 450-NS 3-5 | 34649 | D27256-4 |
| A14710 | 1820-2724 | 0 |  | IC LCH TIL als transparent Octi | 01295 | SN74ALS5 73EN |
| A1U711 | 1820-2724 | 0 |  | IC LCH Ttl als transparent octi | 01295 | SN74ALS573日N |
| A1U712 | 1820-2635 | 2 | 1 | IC GATE TTL ALS AND QUAD 2-INP | 01295 | SN74ALSO8N |
| A11713 | 1820-3100 | 8 | 1 | IC DCDR TTL ALS BIN 3-10-8-LINE 3-INP | 01295 | 2N74ALS138N |
| A1U714 | 1820-2634 | 1 |  | IC INV TTL ALS HEX | 01295 | SN74ALSOABN |
| Alu7is | 1820-2775 | 1 | 1 | IC gate til als nand tpl 3-Inp | 01295 | SNTHALSION |
| A1XU1A1 $\times$ U3- |  |  |  |  |  |  |
| A1 $\mathrm{XU13}$ |  |  |  | NOT ASSIGNED |  |  |
| A1 XU14 A1) XUT5- | 1200-0567 | 1 | 2 | SOCKET-IC 28-CONT OIP-OIP-SLDR | 28480 | 1200-0567 |
| A19 $\times 19$ |  |  |  | NOT ASSIGNED |  |  |
| A1 XU20 | 1200-0654 | 7 | 1 | SOCKET-IC 40-CONT DIP-DIP-SLDR | 28480 | 1200-0654 |
| A1xU21- |  |  |  | NOT ASSIGNED |  |  |
| A $1 \times 3302$ | 1200-0471 | 6 | 1 | SOCKET-IC 8-CONT D8L STRP OIP-SLOR | 28480 | 1200-0471 |
| A1XU303- |  |  |  |  |  |  |
| A $1 \times 4700$ |  |  |  | NOT ASSIGNED |  |  |
| A1 XU703 |  |  |  | NOT ASSIGNED |  |  |
| A1 XU704 | 1200-0639 | 8 | 1 | SOCKET-IC 20-CONT DIP OIP-SLDR | 28480 | 1200-0639 |
| A1 X A1 x | $1200-0639$ $1200-0639$ | 8 8 |  | SOCKET-IC 20 -CONT DIP OIP-SLDR SOCKET-IC 20 -CONT DIP DIP-SLDR | 28480 28480 | $1200-0639$ $1200-0639$ |
| Al $\mathrm{xu} \mathbf{7 0 5}$ |  |  |  |  |  |  |
| A1 XU708 A1 $\times 0709$ |  |  |  | NOT ASSIGNED SOCKET-IC 28 -CONT OIP-DIP-SLDR | 28480 | 1200-0567 |
| A1 XU709 | 1200-0567 | 1 |  | SOCKET-IC 28-CONT OIP-DIP-SLOR | 28480 | 1200-0567 |
| AIXYI | 1200-0475 | 0 | 1 | CONNECTOR-SGL CONT SKT . O17-IN-BSC-SZ | 28480 | 1200-0475 |
| A1Y1 | 0410-0423 | 2 | 1 | CRYSTAL-QUARTZ 10.000 MHZ | 28480 | 0410-0423 |
| A1Y2 | 0410-1142 | 4 | 1 | CRYSTAL-QUARTZ $4.00000 \mathrm{MHZ} \mathrm{HC-18/0-HLDR}$ | 28480 | 0410-1142 |
| A1Y701 | 0410-1142 | 4 | 1 | CRYSTAL-QUARTZ 4.00000 MHZ HC-18/U-HLDR | 28480 | 0410-1142 |

Table 6-2. Replaceable Parts (Continued)


See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Continued)


See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Continued)

| Reference Designation | HP Part Number | $\left\lvert\, \begin{aligned} & C \\ & D \end{aligned}\right.$ | Qty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A2DS62 | 1990-0487 | 7 |  | LED-LAMP LUM-INT $=2 M C D$ BVR $=5 \mathrm{~V}$ | 28480 | HLMP - 1401 |
| A20S63 | 1990-0486 | 6 |  | LED-LAMP LUM-INT $=2 \mathrm{MCD}$ IF $=25 \mathrm{MA}-\mathrm{MAX}$ BVR $=5 \mathrm{~V}$ | 28480 | HLMP-1301 |
| A2H1 | 0380-1539 | 8 | 2 | STANDOFF-NYLON 8L M 3.0 | 28480 | 0380-1539 |
| $\mathrm{A}^{\text {2 }} \mathrm{H} 2$ | 0380-1539 | 8 |  | STANDOFF-NYLON 8L M 3.0 | 28480 | 03801539 |
| A2H3 | 0515-0886 | 3 | 2 | SCREW-MACH M3 $\times 0.5$ GMM-LG PAN-HD | 28480 | 0515-0886 |
| ${ }^{\text {A2 }} \mathrm{H} 4$ | 0515-0886 | 3 |  | SCREW-MACH M3 $\times 0.5$ GMM-LG PAN-HO | 28480 | 0515-0886 |
| A2H5 | 0515-0753 | 3 | 2 | SCREU-MACH M3 $\times 0.5$ SMM-LG PAN-HD | 00000 | ORDER BY DESCRIPTION |
| A2H6 | 0515-0753 | 3 |  | SCREW-MACH M3 $\times 0.5$ 5MM-LG PAN-HD | 00000 | ORDER GY DESCRIPTION |
| A2H7 | 05334-00015 | 6 | 1 | SUBPANEL-LED | 28480 | 05334-00015 |
| A2J1 | 1251-2026 | 8 | 1 | CONNECTOR-PC EDGE 18-CONT/ROW 2-ROWS | 28480 | 1251-2026 |
| $\begin{aligned} & \text { A2MP1- } \\ & \text { A2MP29 } \end{aligned}$ |  |  |  | NOT ASSIGNED |  |  |
| A2MP30 | 5041-0285 | 6 | 14 | KEY CAP PRL GLP | 28480 | 5041-0285 |
| A2mP31 | 5041-0285 | 6 |  | KEY CAP PRL GLP | 28480 | 5041-0285 |
| A2MP32 | 5041-0285 | 6 |  | KEY CAP PRL GLP | 28480 | 5041-0285 |
| A2MP33 | 5041-0285 | 6 |  | KEY CAP PRL GLP | 28480 | 5041-0285 |
| A2MP34 | 5041-0285 | 6 |  | KEY CAP PRL GLP | 28480 | 5041-0285 |
| A2mp3s | 5041-0285 | 6 |  | KEY CAP PRL GLP | 28480 | 5041-0285 |
| A2MP3 ${ }^{\text {a }}$ | 5041-0285 | 6 |  | KEY CAP PRL GLP | 28480 | 5041-0285 |
| A2MP37 | 5041-0285 | 6 |  | KEY CAP PRL GLP | 28480 | 5041-0285 |
| A2MP38 | 5041-0285 | 6 |  | KEY CAP PRL GLP | 28480 | 5041-0285 |
| A2MP39 | 5041-0285 | 6 |  | KEY CAP PRL GLP | 28480 | 5041-0285 |
| A2MP40 | 5041-0285 | 6 |  | KEY CAP PRL GLP | 28480 | 5041-0285 |
| A2MP41 | -5041-0285 | ¢ 6 |  | KEY CAP PRL GLP KEY CAD PRL GLP | 28480 | $5041-0285$ $5041-0285$ |
| A2MP42 | 5041-0285 | 6 |  | KEY CAP PRL GLP | 28480 | 5041-0285 |
| A2MP43 | 5041-0285 | 6 |  | KEY CAP PRL GLP | 28480 | 5041-0285 |
| A2MP44 | 5041-0318 | 6 | 2 | KEY CAP PUT GLP | 28480 | 5041-0318 |
| A2MP45 | 5041-0318 | 6 |  | KEY CAP PUT GLP | 28480 | 5041-0318 |
| A2MP46 |  |  |  | NOT ASSIGNED |  |  |
| A2MP47 |  |  |  | NOT ASSIGNED |  |  |
| A2MP48 | 5041-0342 | 6 | 1 | KEY CAP SG Qtr | 28480 | 5041-0342 |
| A2MP49 |  |  |  | NOT ASSIGNED |  |  |
| A2MP50 | 5041-0351 | 7 | 13 | KAY CAP QUARTER | 28480 | 5041-0351 |
| A2MP5 1 | 5041-0351 | 7 |  | KAY CAP Quarter | 28480 | 5041-0351 |
| A2MPS2 | 5041-0351 | 7 |  | KAY CAP QUARTER | 28480 | 5041-0351 |
| A2MPS 3 | 5041-0351 | 7 |  | Kay cap quarter | 28480 | 5041-0351 |
| A2MP54 | 5041-0351 | 7 |  | KAY CAP QUARTER | 28480 | 5041-0351 |
| A2MP55 | 5041-0351 | 7 |  | Kay cap quarter | 28480 | 5041-0351 |
| A2MP56 | 5041-0351 | 7 |  | KAY CAP Quarter | 28480 | 5041-0351 |
| A2MPS 7 | 5041-0351 | 7 |  | Kay cap quarter | 28480 | 5041-0351 |
| A2MPS8 | 5041-0351 | 7 |  | kay cap quarter | 28480 | 5041-0351 |
| A2MP59 | 5041-0351 | 7 |  | Kay cap quarter | 28480 | 5041-0351 |
| A2MP60 | 5041-0351 | 7 |  | Kay cap quarter | 28480 | 5041-0351 |
| A2MP61 | 5041-0351 | 7 |  | Kay cap quarter | 28480 | 5041-0351 |
| A2MP62 | 5041-0351 | 7 |  | Kay cap quarter | 28480 | 5041-0351 |
| A2MP63 | 5041-0450 | 7 | 1 | KEY CAP blu Qtr | 28480 | 5041-0450 |
| A2MP64 | 5041-0483 | 6 | 1 | 1/4 KEY | 28480 | 5041-0483 |
| A2R1 | 2100-4083 | 3 | 2 | RESISTOR-VAR CONTROL CCP 10K 10\% LIN | 28480 | 2100-4083 |
| A2R2 | 2100-4083 | 3 |  | RESISTOR-VAR CONTROL CCP 10K 10\% LIN | 28480 | 2100-4083 |
| A2S 1 | 5060-9436 | 7 | 32 | PUSHBUTION SWIICH P.C. MOUNT | 28480 | 5060-9436 |
| A2S2 | 5060-9436 | 7 |  | PUSHBUTTON SUITCH P.C. MOUNT | 28480 | 5060-9436 |
| A2S3 | 5060-9436 | 7 |  | PUSHEUTTON SWITCH P.C. MOUNT | 28480 | 5060-9436 |
| A2S4 | 5060-9436 | 7 |  | PUSHBUTTON SUITCH P.C. MOUNT | 28480 | 5060-9436 |
| A2S5 | 5060-9436 | 7 |  | PUSHBUTTON SWITCH P.C. MOUNT | 28480 | 5060-9436 |
| A2S6 A2S | 5060-9436 | 7 |  | PUSHBUTTON SWITCH P.C. MOUNT NOT ASSIGNED | 28480 | 5060-9436 |
| A258 |  |  |  | NOT ASSIGNED |  |  |
| A259 | 5060-9436 | 7 |  | PUSHBUTION SUITCH P.C. MOUNT | 28480 | 5060-9436 |
| A2S 10 | 5060-9436 | 7 |  | PUSHBUTION SWITCH P.C. MOUNT | 28480 | 5060-9436 |
| A2S11 | 5060-9436 | 7 |  | PUSHBUTTON SWITCH P.C. MOUNT | 28480 | 5060-9436 |
| A2S12 | 5060-9436 | 7 |  | PUSHBUTTON SWITCH P.C. MOUNT | 28480 | 5060-9436 |
| A2S 13 | 5060-9436 | 7 |  | PUSHEUTION SUITCH P.C. MOUNT | 28480 | 5060-9436 |
| A2S14 | 5060-9436 | 7 |  | PUSHBUTTON SUITCH P.C. MOUNT | 28480 | 5060-9436 |
| A2S 15 | 5060-9436 | 7 |  | PUSHEUTTON SWITCH P.C. MOUNT | 28480 | 5060-9436 |

See introduction to this section for ordering information

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Table 6-2. Replaceable Parts (Continued)


Table 6-2. Replaceable Parts (Continued)


See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Continued)


See introduction to this section for ordering information *Indicates factory selected value

Table 6-3. Manufacturers Code List



Figure 6-1. HP 5334B Exploded View


Figure 6-2. Front View


Figure 6-3. Rear View

# SECTION 7 <br> MANUAL CHANGES 

## 7-1. INTRODUCTION

7-2. This section contains information necessary to adapt this manual to apply to older instruments.

## 7-3. MANUAL CHANGES

7-4. This manual has been written for, and applies directly to, instruments with serial prefix 2937A.
7-5. As engineering changes are made, newer instruments may have serial prefix numbers higher than the one shown on the title page of this manual. The manuals for these instruments will be supplied with MANUAL CHANGES sheets containing the required information. Replace affected pages or modify existing manual information as directed in the MANUAL CHANGES pages. Contact the nearest Hewlett-Packard Sales and Support Office (listed at the back of this manual), if the change information is missing.

Table 7-1. HP 5334B Backdating

| If Your Instrument has Serial Number | Make the Following Changes to Your Manual |
| :---: | :---: |
| A1 Date Code 88441 | 1 |
| 2937 A | 1,2 |
| 2839A (A1 Date Code 88393) | 1 thru 3 |
| 2826 A | 1 thru 4 |
| 2704A00147 thru 2804A00838 | 1 thru 5 |
| 2704A00117 thru 2704A00146 | 1 thru 6 |

## CHANGE (1) A1 DATE CODE 88441

Table 6-1, Replaceable Parts:
Change A1 (05334-60014, -60015, -60017, -60018) Date Code to 88441
Delete the asterisk $\left(^{*}\right)$ at A1C5, indicating factory-selected value.
Delete A1C5*, 0160-3875, CAPACITOR-FXD 22PF +5\% 200VDC CER $0+30$.
Delete A1C5*, 0160-4386, CAPACITOR-FXD 33PF + 5\% 200VDC CER 0+30.
Delete A1C5*, 0160-4492, CAPACITOR-FXD 18PF + $5 \%$ 200VDC CER 0+30.
Delete A1C5*, 0160-4493, CAPACITOR-FXD 27PF +5\% 200VDC CER 0+30.
Page 103, Figure 8-24. P/O A1 Main Board Timebase/Power Supply Blocks Schematic Diagram/Component Locator (Sheet 5 of 7):
Change A1 SERIES at top of schematic to Date Code 88441.
Delete the asterisk (*) at A1C5, indicating factory-selected value.

CHANGE (2) SERIES 2937A
Table 6-2, Chassis Parts:
Change MP9 from 5001-0538 to 5001-0438, TRIM-SIDE.
Change MP10 from 5041-8801 to 5040-7201, FOOT.
Change MP11 from 5041-8802 to 5040-7202, TOP TRIM.
Change MP12 from 5041-8819 to 5041-6819, STRAP-HANDLE CAP FR.
Change MP13 from 5041-8820 to 5041-6820, STRAP-HANDLE CAP R.
Change MP14 from 5062-3702 to 5060-9802, STRAP-HANDLE ASSY.
Change MP21 from 05334-00025 to 05334-00021, COVER-OUTER.
Change MP23 from 05334-20203 to 05334-20201, FRAME-FRONT MOD.

CHANGE (2) SERIES 2937A (Continued):
Table 6-2. Option Parts:
Change Option 907 HANDLE-FRONT KIT from 5062-3988 to 5061-9688.
Change Option 908 RACK FLANGE KIT from 5062-3974 to 5061-9674.
Change Option 909 RACK/HANDLE KIT from 5062-3975 to 5061-9675.

CHANGE (3) SERIES 2839A (A1 DATE CODE 88393)
Table 6-1. A1 Main Board Assembly Replaceable Parts:
Change A1 (05334-60014, -60015,-60017, -60018) Date Code to 88393.
Delete A1C9, 0160-0576 CAPACITOR .1UF.
Change A1C81 from 0160-4386 (33PF) to 0160-5603 CAPACITOR-FXD 33PF $\pm 5 \% 500 \mathrm{VDC}$ CER $0 \pm 30$.
Change A1C88 from 0160-4527 (56PF) to 0160-5602, CAPACITOR-FXD 56PF $+5 \% 500 \mathrm{VDC} \mathrm{CER} \mathbf{0}+30$.
Delete A1C105, C106, 0160-4554 CAPACITOR-FXD .01UF + -20\% 50VDC CER.
Change A1J204 from 1251-7136 to 1251-5418 to CONNECTOR-PC EDGE 15-CONT /ROW 2-ROWS.
Add A1R15, 0698-3442 RESISTOR 237 1\% .125W F TC=0+-100.
Delete A1R134, 0757-0394 RESISTOR $51.11 \%$. 125 W TF TC=0+-100.
Delete A1R135, 1810-0203 RESISTOR-NETWORK 8-SIP 470.0 OHM X 7.
Change TP1/TP21 from 0360-0124 to 1251-4707 CONNECTOR-SGL CONTACT .031-IN-BSC SZ.
Add A1XU14, 1200-0567, SOCKET-IC 28-CONT DIP.
Add A1XY1, 1200-0475 CONNECTOR-SGL CONT SKT.
Figure 8-20. P/O Main Board Input Amplifier Block Schematic Diagram/Component Locator (Sheet 1 of 7): Change A1 SERIES at top of schematic to Date Code 88393.

Figure 8-21. P/O Main Board DAC Block Schematic Diagram/Component Locator (Sheet 2 of 7):
Change A1 SERIES at top of schematic to Date Code 88393.
Figure 22. P/O A1 Main Board Executive/Meas Block Schematic (Sheet 3 of 7):
Change A1 SERIES at top of schematic to Date Code 88393.
Figure 8-23. P/O A1 Main Board HP-IB Block Schematic Diagram (Sheet 4 of 7):
Change A1 SERIES at top of schematic to Date Code 88393.
Figure 8-24. P/O A1 Main Board Timebase/Power Supply Blocks Schematic Diagram/Component Locator (Sheet 5 of 7 )
Change A1 (05334-60014, -60015, -60017, -60018) Date Code 88393.
Replace the A1 component locator with A1 component locator (Date Code 88393) supplied in this manual backdating section.
Replace the " 10 MHz ECL Crystal Oscillator" portion of the schematic (upper left) with the following:


Figure 8-24. P/O A1 Main Board Timebase/Power Supply Schematic Diag/Component Locator (Sheet 5 of 7): Change A1 (05334-60014, -60015, -60017, -60018) to Date Code 88393.
Replace part of the Power Supply portion of the schematic (center) with the following:


Figure 8-26. P/O A1 Main Board Option 030 Channel C Block Schematic (Sheet 7 of 7): Change A1 (05334-60014, -60015, -60017, -60018 ) Date Code to 88393.

## CHANGE (4) SERIES 2826A

Table 6-2. A2 Front Panel Board Assembly Replaceable Parts:
Change A2MP44/MP45 from 5041-0285 to 5041-0318 (Color change from light to medium gray.)
Table 6-2. Chassis Parts:
Change 2360-0209 to 2360-0129 SCREW-MACHINE 6-32 1-IN-LG PAN-HD POZI.
Delete 2190-0006, WASHER-LOCK.

## CHANGE (5) (2704A00147 thru 2804A00838)

Make this change for instruments that contain the Revision B and C, A1 Main Board Assembly.
Table 6-2, Replaceable Parts:
Delete A1C103, 0180-3775, CAPACITOR-FXD 3300UF + $30-10 \%$ 16VDC AL.
Delete A1C104, 0160-0576, CAPACITOR-FXD .1UF $\pm 20 \%$ 50VDC CER.
Delete A1CR40, 1902-0951, DIODE-ZNR 5.1V 5\% DO-35 PD $=.4 \mathrm{~W}$ TC $=+.065 \%$
Delete A1R142, 0698-0082, RESISTOR $4641 \%$. 125 W F TC=0 $=100$.
Delete A1R143, 2100-4158, RESISTOR-TRIM 10K 10\% TKF TOP ADJ-25-TRN
Delete A1R144, 0757-0290, RESISTOR 6.19K $1 \%$. 125 W F TC=0+100.
Delete A1R331, 0757-0280, RESISTOR 1K 1\% .125W F TC=0 +100 .
Change A1R291 and R295 from 0757-0465 (100K) to 0757-0465, RESISTOR 100K $1 \% .125 \mathrm{~W}$ F TC=0 0100 .
Change A1R293 from 0757-0433 (11K) to 0757-0443, RESISTOR 11K $1 \% .125 \mathrm{~W}$ F TC=0 $\pm 100$.
Delete A1R294, 0757-0199, RESISTOR 21.5K 1\% .125W F TC=0 +100 .
Delete A1U292, 1826-1338, IC MISC 8-DIP-P PKG.
Add A1U291, 1826-0412, IC COMPARATOR PRCN DUAL 8-DIP-PKG.
Paragraph 8-218. Power-up RESET Circuit Description:
Change paragraph 8-219 to read as follows:
8-219. The RESET circuit U291, is a comparator with an open collector output that synchronizes the HP-IB MCU (U17), Measurement MCU (U19), and MATE Microprocessor (U702). U291 also keeps the reset lines low for a minimum of 100 ms . The 100 ms delay allows the clock in the HP-IB MCU time to stabilize. Resistors R293 and R294 form a voltage-divider that applies approximately 3 volts to the plus side of U291A (pin 3). Resistor R291 and capacitor C709 provide an RC time constant that applies a rising voltage to the negative side of U291A (pin 2). The rising voltage on pin 2 equals the voltage on pin 3 in approximately 100 ms When the voltage on the negative input goes above the voltage on the positive input, the output (pin 1) goes LOW. When pin 1 goes LOW, pin 7 of U291B goes HIGH and resets the HP-IB MCU, Measurement MCU, and MATE Microprocessor.

Figure 8-19. HP 5334B Component Locator:
Delete C103, C104, CR40, R142, R144, and R143, which are the components of the Oven Oscillator
Fine Adjust circuit located near the Option 010 Oven Oscillator.

CHANGE (5) (2704A00147 thru 2804A00838)
Figure 8-23. P/O A1 Main Board HP-IB Schematic Block Diagram:
Change the SERIES number from 2804 to 2704.
Change the POWER-UP RESET circuit as shown in the following figure:


Figure 8-24. P/O A1 Main Board Timebase/Power Supply Blocks Schematic Diagram:
Change the SERIES number from 2804 to 2704.
Delete C103, C104, CR40, R142, R143, and R144 of the OVEN OSCILLATOR FINE ADJ circuit. Delete the EFC and EFC GND input lines of the OVEN OSCILLATOR FINE ADJ circuit.

Figure 8-26. P/O A1 Main Board Option 030 Channel C Block Schematic Diagram:
Change the SERIES number from 2804 to 2704.
Delete R331.

CHANGE (6) (2704A00117 thru 2704A00146)
Make this change for instruments that contain the Revision B, only, A1 Main Board Assembly.

Table 6-2. Replaceable Parts:
Delete A1R211, 0698-3432, RESISTOR $26.1 \% .125 \mathrm{~W}$ F TC=0 $\mathbf{+ 1 0 0}$.
Figure 8-19. HP 5334B Component Locator:
Delete R211

Figure 8-20. P/O A1 Main Board Input Amplifier Block Schematic Diagram:
Delete R211.

## 8-1. INTRODUCTION

8-2. This section contains circuit descriptions, troubleshooting information, block diagram, schematics and component locators for the HP Model 5334B Universal Counter.

## 8-3. SAFETY CONSIDERATIONS

8-4. Although the HP 5334B has been designed in accordance with international safety standards, this section has information, cautions, and warnings that must be followed to ensure safe operation and to keep the instrument in a safe condition.
WARNING
MAINTENANCE DESCRIBED IN THIS SECTION IS PERFORMED WITH
POWER SUPPLIED TO THE INSTRUMENT AND PROTECTIVE COVERS
REMOVED. THIS MAINTENANCE SHOULD BE PERFORMED ONLY BY
QUALIFIED SERVICE PERSONNEL WHO ARE AWARE OF THE
HAZARDS INVOLVED (FOR EXAMPLE, FIRE AND ELECTRICAL
SHOCK). WHERE MAINTENANCE CAN BE PERFORMED WITHOUT
POWER APPLIED, THE INSTRUMENT SHOULD BE DISCONNECTED
FROM ITS POWER SOURCE.

WARNING
ALL PROTECTIVE EARTH TERMINALS, EXTENSION CORDS, aUtotransformers, and devices connected to the COUNTER MUST BE CONNECTED TO A PROTECTIVE EARTH grounded socket. any interruption of the protective earth grounding will create a potential shock hazard THAT COULD RESULT IN PERSONAL INJURY.

## WARNING

ONLY 250-VOLT FUSES OF THE SPECIFIED TYPE WITH THE REQUIRED CURRENT RATING SHOULD BE USED. DO NOT USE REPAIRED FUSES OR SHORT CIRCUITED FUSEHOLDERS. TO DO SO COULD CAUSE A SHOCK OR FIRE HAZARD.

8-5. Whenever it is suspected that fuse protection or protective earth grounding has been defeated, the HP 5334B must be disconnected from the power lines and operation must not be allowed until the situation is corrected.

## WARNING

POWER IS ALWAYS PRESENT AT THE POWER SWITCH AND TRANSFORMER, AND DC VOLTAGE IS PRESENT WHENEVER THE POWER CABLE IS CONNECTED TO THE AC POWER LINES. THE POWER CORD MUST BE DISCONNECTED FROM THE INSTRUMENT TO REMOVE ALL POWER FROM THE INSTRUMENT.

8-6. Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its power source.

## 8-7. CIRCUIT DESCRIPTIONS

8-8. The circuit descriptions of the HP 5334B Counter are divided according to functional blocks. The description of each block is presented in two parts. First, an overall explanation is given of the particular section (Theory of Operation, paragraphs 8-70 through 8-101). And, second, a more detailed component-level description is provided (Detailed Theory of Operation, paragraphs 8-102 through 8-279).

## 8-9. TROUBLESHOOTING

## 8-10. General

8-11. Troubleshooting for the HP 5334B is designed to help the service technician find the component causing the instrument to to fail. To accomplish this, two types of troubleshooting methods are used: (1) Signal Tracing, and (2) Signature Analysis.

## 8-12. Signal Tracing

8-13. This type of troubleshooting employs the traditional methods of using a voltmeter and oscilloscope to measure signal amplitude and observe waveforms. The bulk of the troubleshooting information provided here uses signal tracing.

## 8-14. Signature Analysis

8-15. Signature Analysis is a simple method of verifying the operation of digital circuitry. When properly used, signature analysis can detect extremely subtle hardware faults. Signatures must identically match those given in the Signature Analysis section which follows Signal Tracing. If everything is working correctly, signatures will all match exactly. If they do not match, by even one digit, something is wrong.

8-16. With the Counter's internal signature analysis routine, the signature analyzer's test probe is used to check nodes in the circuit under test. The signature analyzer converts the signals at the node into a four digit "signature", which it displays. The signature is then compared to the corresponding one from the printed list of signatures. These two signatures must be identical.

8-17. Signature analysis can be performed more efficiently if the following considerations are kept in mind:
a. Make sure that every step is performed as described in the setup procedure. That is, make sure that the clock, start, and stop connections and triggering are correct.
b. Double check that the signatures are being taken at the correct node.
c. Make sure that the signature analyzer probe is making good contact with the pin being checked. Oxidation on pins can cause invalid signatures due to poor contacts.
d. When you think that you have found a bad signature, double check to make sure.
e. When checking a node, check that the unstable signature indicator is not blinking.

## 8-18. RECOMMENDED TEST EQUIPMENT

8-19. Table $1-5$ lists the recommended equipment for the service procedures. If the specified equipment is not available, other equipment may be used if its performance meets the critical specifications listed in Table 1-5. Note that an HP 8565A Spectrum Analyzer ( $500 \mathrm{MHz}-18 \mathrm{GHz}$ ) is needed to troubleshoot the 30 dB Amplifier circuit in the Channel C Input Block.

## 8-20. SERVICE TOOLS AND AIDS

## 8-21. Parts Locations

8 -22. The locations of individual components mounted on printed circuit boards or other assemblics are shown adjacent to the appropriate schematic sheet. The part reference designation is the assembly designator plus the part designator. For example, A1R9 is on the A1 assembly. For specific component descriptions and ordering information, refer to Section VI, Replaceable Parts. Chassis and frame parts, including mechanical parts, are also identified in Section VI.

## 8-23. Adjustment and Test Point Locations

8-24. Adjustment locations are shown in the adjustment procedures of Section V. Adjustable components and test points can be found on the component locator figure opposite the particular assembly's schematic sheet.

## 8-25. Service Aids on Printed Circuit Boards

8 -26. The service aids on printed circuit boards include test points and integrated circuit designations. These component reference designators are printed onto the A1 Main Board and are reference on the schematic diagram as well. Test points are provided for measuring signals at several points in a circuit.

## 8-27. Pozidriv Screwdrivers

8-28. Many screws in the HP 5334B appear to be Phillips screws, but are not. To avoid damage to the screw slots, Pozidriv screwdrivers should be used.

## 8-29. REPAIRS

## 8-30. Cleaning Printed-Circuit Boards

8-31. After soldering a component to a printed-circuit (PC) board, HP recommends that you DO NOT remove the flux from the soldered area. It has been found that after a hand soldering operation, the solder flux from RMA-P2 (Rosin, Mildly Active) solder does no harm if left in place on a PC board; the flux residue is inert and nonconductive. However, when the flux is dissolved with a chemical, in an attempt to remove it from the board, it spreads over the board, releasing several activators (chlorides, bromides, etc.). Now, instead of having a harmless flux residue with the water soluble activators trapped inside, you have a potential corrosion problem. If the instrument is stored in a humid environment, over time moisture will be absorbed which can start the corrosion process.

## 8-32. Disassembly and Reassembly Procedures

8-33. Procedures for removal and installation of the cover and chassis are described in paragraphs 8-280 through 8-286. Procedures for removal and installation of the Front Panel assembly are described in paragraphs 8-287 through 8-290. Also, disassembly procedures for troubleshooting the internal components of the Option 010 Oven Oscillator are described in paragraphs 8-397 through 8-399. For procedures on field installations of Option 010 Oven Oscillator, refer to paragraph 8-475.

## 8-34. Post-Repair Adjustments

8-35. Table 5-2 describes the adjustment procedures that are related to repair or replacement of a functional block of the instrument.

## 8-36. Post-Service Product Safety Checks

8-37. Visually inspect interior of instrument for any signs of abnormal internally generated heat, such as discolored printed circuit boards or components, damaged insulation, or evidence of arcing. Determine and remedy cause of any such condition.

8-38. Using a suitable ohmmeter, check resistance from instrument enclosure to ground pin on power cable plug. The reading must be less than one ohm. Flex the power cable while making this measurement to determine whether intermittent discontinuities exist.

8-39. Check any indicated front or rear panel ground terminals marked, using the above procedure.
8-40. Check resistance from instrument enclosure to line and neutral (tied together) with the power switch ON and the power source disconnected. The minimum acceptable resistance is two Megohms. Replace any component which results in a failure.

## 8-41. SCHEMATIC DIAGRAM NOTES

$8-42$. Figure 8-1 shows the symbols used on the schematic diagrams. This same figure also shows the method of assigning reference designators, assembly numbers, and subassembly numbers.

## 8-43. Reference Designations

8-44. Assemblies such as printed circuit boards are assigned numbers in sequence, A1, A2, etc. Reference designators for individual components are determined by adding the assembly number as a prefix for component number. For example, the complete reference designation for U1 on assembly A1 is A1U1.

## 8-45. Identification Marks on Printed Circuit Boards

8-46. HP printed circuit boards, as shown in Figure 8-1, have four identification numbers: an assembly part number, a series number, a revision letter, and a production code. The assembly part number consists of 10 digits (such as 05334-60016) and is the primary identification. All assemblies with the same part number are interchangeable. When a production change is made on an assembly that makes it incompatible with previous assemblies, a change in part number is required.

8-47. The series number (such as 2844) is used to document minor electrical changes. As changes are made, the series number is incremented. When replacement boards are ordered, you may receive a replacement with a different series number. If there is a difference between the series number stamped on the board and the schematic in this manual, a minor electrical difference exists. If the number on the printed circuit board is lower than that on the schematic, refer to Section VII for backdating information. If it is higher, manual change information will be provided with this manual. If the manual change sheets are missing, contact your nearest HP Sales and Support Office. Refer to the listing at the back of this manual.

8-48. Revision letters ( $A, B$, etc.) denote changes in printed circuit layout. For example, if a capacitor type is changed (electrical value may remain the same) and requires different spacing for its leads, the printed-circuit board layout is changed and the revision letter is incremented to the next letter. When a revision letter changes, the series number is also usually changed. The production code is the four digit seven-segment number used for production purposes.


Figure 8-1. Schematic Diagram Notes
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## 8-49. LOGIC SYMBOLS

8-50. Logic symbols used in this manual conform to the American National Standard ANSI/IEEE Std. 91-1984. This standard supersedes MIL-STD-806B. Tables 8-1 through 8-6 give a brief summary of the symbols used for logic devices, and the associated qualifiers and indicators. Not all of the symbols listed have been used in this manual, but they are included in the tables for the sake of completeness.*

## 8-51. General Qualifying Symbols

8-52. Table 8-1 shows the characters generally used to define the basic function of a device represented by a logic symbol or element. The characters are placed near the top center or geometric center of the symbol or symbol element.

Table 8-1. General Qualifying Symbols

| Symbol | Description | Example |
| :---: | :---: | :---: |
| \& | AND gate or function. | SN7400 |
| $\geq 1$ | OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output. | SN7402 |
| $=1$ | Exlusive OR. One and only one input must be active to activate the output. | SN7486 |
| $=$ | Logic identity. All inputs must stand at same state. | SN74180 |
| 2 k | An even number of inputs must be active. | SN74180 |
| $2 \mathrm{k}+1$ | An odd number of inputs must be active. | SN74ALS86 |
| 1 | The one input must be active. | SN7404 |
| $\triangleright$ or $\triangleleft$ | A buffer or element with more than usual output capability (symbol is oriented in the direction of signal flow). | SN74S436 |
| $\square$ | Schmitt trigger; element with hysteresis. | SN74S18 |
| $X Y$ | Coder, code converter (DEC/BCD, BIN/OUT, BIN/7-SEG, etc.). | SN74LS347 |
| MUX | Multiplexer/data selector. | SN74150 |
| DMUX or DX | Demultiplexer. | SN74138 |
| $\Sigma$ | Adder. | SN74LS385 |
| P-Q | Subtracter. | SN74LS385 |
| CPG | Look-ahead carry generator. | SN74182 |
| $\pi$ | Multiplier. | SN74LS384 |
| COMP | Magnitude comparator. | SN74LS682 |
| ALU | Arithmetic logic unit. | SN74LS381 |
| $\Omega$ | Retriggerable monostable. | SN74LS422 |
| $1 \Omega$ | Non-retriggerable monostable (one-shot). | SN74121 |
| $\Omega$ | Astable element. Showing waveform is optional. | SN74LS320 |
| $\stackrel{!}{G}$ | Synchronously starting astable. | SN74LS624 |
| $\stackrel{\mathrm{G!}}{\square}$ | Astable element that stops with a completed pulse. | - |

Table 8-1. General Qualifying Symbols (Continued)

| Symbol | Description | Example |
| :---: | :--- | :---: |
| SRGm | Shift register. $m=$ number of bits. | SN74LS595 |
| CTRm | Counter. $m=$ number of bits; cycle length $=2^{m}$. | SN54LS590 |
| CTR DIVm | Counter with cycle length $=m$. | SN74LS668 |
| RCTRm | Asynchronous (ripple-carry) counter; cycle length $=2^{m}$. | $\bullet$ |
| ROM | Read-only memory. | SN74187 |
| RAM | Random-access read/write memory. | SN74170 |
| FIFO | First-in, firt-out memory | SN74LS222 |
| I $=0$ | Element powers up cleared to 0 state. |  |
| $\Phi$ | Highly complex function; "gray box" symbol with limited detail shown <br> under special rules. | SN74AS877 |

## 8-53. Gate Symbols

8-54. The ANSI/IEEE standard defines new symbols for the basic gate functions, but also permits the use of the MIL-STD-806B symbols for these gates, as shown in Figure 8-2. In this manual, the distinctively shaped ANDgate, OR-gate, Exclusive-OR-gate, and Inverter symbols will be used for those gates which are not part of a complex logic device. The new symbols will be used for those gates embedded within a logic symbol, signifying that they are one element of more complex logic device.


Figure 8-2. Gate Symbols

## 8-55. Qualifying Symbols for Inputs and Outputs

8-56. The symbols shown in Table 8-2 are used to indicate the external states of both gate and complex logic devices, and their relationship to internal states.

Table 8-2. Qualifying Symbols for Inputs and Outputs

| Logic negation at input. External 0 produces internal 1. |
| :--- | :--- |
| Logic negation at output. Internal 1 produces external 0. |
| Active-low input. |
| Active-low output. |
| Active-low output in the case of right-to-left signal flow. |
| Signal flow from right-to-left. If not otherwise indicated, signal flow is from left-to-right. |
| Bynamic input. The transition from the external 0 state to the external 1 state |
| produces a transitory internal 1 state. At all other times, the internal logic state is 0. |
| Nonlogic connection. A label inside the device symbol will usually define the nature |
| of the input or output. |
| Analog input or output. |

## 8-57. Qualifying Symbols for Internal Connections

8-58. The internal connections between elements abutted together in a logic symbol are indicated by the symbols shown in Table 8-3. Note that the internal (virtual) input is an input originating somewhere else in the device and is not connected directly to a pin. The internal (virtual) output is likewise not connected to a pin.

Table 8-3. Qualifying Symbols for Internal Connections

| Symbol | Description |
| :---: | :---: |
|  | Internal connection. 1 state on left produces 1 state on right. <br> Negated internal connection. 1 state on left produces 0 state on right. <br> Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right. <br> Internal input (virtual input). It always stands at its internal 1 state unless affected by an overriding dependency relationship. <br> Internal output (Virtual output). Its affecft on an internal input to which it is connected is indicated by dependency notation. |

## 8-59. Symbols Inside the Outline

8-60. Table 8-4 shows some of the symbols used inside the outline of a logic symbol. Note particularly that opencollector, open-emitter, and three-state outputs have distinctive symbols. Also note that an EN (Enable) input affects all the outputs of the circuit and has no affect on inputs. When an Enable input affects only certain outputs and/or affects one or more inputs, a form of dependency notation will indicate this (refer to paragraph 8-61).

Table 8-4. Symbols Inside the Outline

| Symbol | Description |
| :---: | :---: |
| $\neg$ - | Postponed output (of a pulse-triggered flip-flop). The output changes when input initiating change (e.g., a C input) returns to its initial external state or level. |
| -10 | Bi-threshold input (input with hysteresis) |
| 나 | NPN open-collector or similar output that can supply a relatively low-impedance $L$ level when not turned off. Requires external pull-up. Capable of positive-logic wiredAND connection. |
| $\theta$ - | Passive-pull-up output is similar to NPN open-collector output but is supplemented with a built-in passive pull-up. |
| 하 | NPN open-emitter or similar output that can supply a relatively low-impedance $H$ level when not turned off. Requires external pull-down. Capable of positive-logic wired-OR connection. |
| 하 | Passive-pull-down output is similar to NPN open-emitter output but is supplemented with a built-in passive pull-down. |
| 마 | 3 -state output |
| 1 | Output with more than usual output capability (symbol is oriented in the direction of signal flow). |
| - | Enable input <br> When at its internal 1-state, all outputs are enabled. When at its internal 0 -state, open-collector and open-emitter outputs are off, 3 -state outputs are at normally defined internal logic states and at external high-impedance state, and all other outputs (e.g., totempoles) are at the internal 0 -state. |
| J, K, R, S. T | Usual meanings associated with flip-flops (e.g., $\mathrm{R}=$ reset, $\mathrm{T}=$ toggle). |
| $-10$ | Data input to a storage element equivalent to: $\square_{R}^{s}$ |
| $\rightarrow \rightarrow m-m$ | Shift right (left) inputs, $m=1,2,3$ etc. If $m=1$, it is usually not shown. |
| $\xrightarrow{-1}+-\mathrm{m}$ | Counting up (down) inputs, $m=1,2,3$ etc. If $m=1$, it is usually not shown. |
| [ ${ }^{\circ}$ | Binary grouping. $m$ is highest power of 2 . |
| $-\backslash \mathrm{CT}=15$ | The contents-setting input, when active, causes the content of a register to take on the indicative value. |
| $\mathrm{CT}=9 \vdash$ | The content output is acftive if the content of the register is as indicated. |
| 1] | Input line grouping . . . indicates two or more terminals used to implement a single logic input. |
|  | e.g., The paired expander inputs of SN7450. ${ }_{\sim}^{x}$ - |
| "1" | Fixed-state output always stands at its internal 1 state. For example, see SN74185. |

## 8-61. Dependency Notation

8-62. Dependency notation is a way to simplify symbols from complex IC elements by denoting the relationship between inputs, outputs, or inputs and outputs, without actually showing all the elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function. Table 8-5 contains a summary of the 11 types of dependency notations.

Table 8-5. Summary of Dependency Notation

| Type of Dependency | Letter Symbol* | Affecting Input At lis 1-State | Affectting Input At lts 0-State |
| :---: | :---: | :---: | :---: |
| Address | A | Permits action (address selected). | Prevents action (address not selected). |
| Control | C | Permits action. | Prevents action. |
| Enable | EN | Permits action. | Pervents action of inputs. outputs off. outputs at external high impedance, no change in internal logic state. Other outputs at internal 0 state. |
| AND | G | Permits action. | Imposes 0 state. |
| Mode | M | Permits action (mode selecfted). | Prevents action (mode not selected). |
| Negate (X-OR) | N | Complements state. | No effect. |
| RESET | R | Affected output reacts as it would to $S=0, R=1$. | No effect. |
| SET | S | Affected output reacts as it would to $S=1, R=0$. | No effect. |
| OR | V | Imposes 1 state. | Permits action. |
| Transmission | X | Bidirectionally connected input to output. | Input to output bidirectionally not connected. |
| Interconnection | Z | Imposes 1 state. | Imposes 0 state. |
| *These letter symbols appear at the AFFECTING input (or output) and are followed by a number. Each input (or output) AFFECTED by that input is labeled with that same number. When the labels EN, R, and S appear at inputs without the following numbers, the descriptions above do not apply. The action of these inputs is described under "Symbols Inside the Outine". |  |  |  |

8-63. Table $8-6$ contains examples of dependency notation using the " $G$ " (AND) and " $C$ " (Control) dependency symbols. Refer to the ANSI/IEEE Std. 91-1984 for a complete explanation of dependency notation.

Table 8-6. Examples of Dependency Notation


## 8-64. Control Blocks

8 -65. A common control block is often used in conjunction with an array of related elements. (See Figure 8-3.) A control block is the point of placement for inputs and outputs associated with more than one element of the array, or with no element of the array. Such inputs and outputs will be labeled when appropriate. Refer to paragraph 8-66 for an example of the use of control blocks.


Figure 8-3. Common Control Block

## 8-66. Logic Device Notation Example

8-67. The various logic symbols are combined to represent more complex devices that perform more difficult functions. The control block symbol can simplify understanding of many complex devices. An example of such a device is given here. This example is typical of the symbols used in the schematic diagrams in this manual.

This device is used as an interface between an external controller and the HP-IB microcomputer on the Data Bus.

In this example, G1 controls both EN2 and EN3. The logic level on pin 11 determines whether data is transmitted or received.

With a LOW at G1 (pin 9), the device is enabled for operation. A HIGH at pin 11 sets the device into the transmit mode and the data on the left-side inputs will pass to the right-side outputs.

A LOW at pin 11 sets the device into the receive mode and the data on the right-side inputs will pass to the left-side outputs.

A HIGH at G1 disables the device (by driving all inputs and outputs to a high impedance state) preventing any data transfer.


Figure 8-4. 3-State Bidirectional Transceiver

## 8-68. LOGIC LEVELS

8-69. This instrument uses three types of device logic. They are:
a. Transistor-Transistor Logic (TTL).
b. Emitter-Coupled Logic (ECL).
c. Emitter-Function Logic (EFL).

Shown below are the High and Low logic levels associated with each type of logic. The values are approximate.

Table 8-7. Logic Levels

| LOGIC STATE | TTL | ECL | EFL |
| :---: | :---: | :---: | :---: |
| HIGH | +2.0 V to +5.0 V | -0.9 V | +2.1 V |
| LOW | 0 V to +0.8 V | -1.8 V | +1.5 V |

## 8-70. THEORY OF OPERATION

8-71. The theory of operation describes the general overall operation of the HP 5334B and the operation of each block assembly (circuit) located on the A1 Main board, the A2 Front Panel board, and the Option 010 Oven Oscillator plug-in module.

## 8-72. General

8-73. The overall operation of the HP 5334B is shown in the block diagram, Figure 8-18. The Counter uses three microcomputers (MCU): the Executive MCU for overall control, the Measurement MCU for control of measurement functions, and the HP-IB MCU for control of system interface functions. Each MCU carries out its routines under the direction of its own internally stored program. The overall operation of the counter depends on the continuous interaction of the Multiple-Register Counter (MRC), described in the next paragraph, and the controlling MCU system which centers around the Executive, and Measurement MCUs.

8-74. The MCU system contains the processor, the counter operating program (ROM), and memory space (RAM). The Multiple-Register-Counter (MRC), referred to as a "counter-on-a-chip", is a Large-Scale Integration (LSI) circuit which contains the counting registers used to accumulate the raw input measurement data. The microcomputer system contains the processor, the counter operating program (ROM), and memory space (RAM).

8-75. Inputs to Channel A and/or B are routed through signal conditioning circuits which perform the operator selections of coupling, impedance, and attenuation. These signals are directed to the MRC, where they are accumulated in registers, counted, and stored as raw measurement data. The data is then retrieved by the microcomputer system, manipulated to achieve the desired measurement mode, and routed to the display.

8-76. The Time Base is used as the reference for the counting done by the MRC. An interpolating technique is used that divides up the time between the reference oscillator pulses and allows the MRC to count much finer resolution.

8-77. For a typical measurement, the MCU system reads the MRC registers, reads the interpolator counters, performs the necessary calculations, and displays the result.

8-78. Data is transferred between the MCUs, and to and from the other functional areas over two data buses, the Executive Data Bus and the Measurement Data Bus. Since the data buses are used for communicating with many devices, control lines generate signals to tell selected devices that the data on the bus is intended for them.

8-79. The instrument consists of eleven major functional circuit blocks, listed below:

- Executive Block
- Measurement Block
- Input Amplifier Block
- Digital-to-Analog Converter (DAC) Block
- Time Base Block
- HP-IB Block
- Power Supply Block
- Channel C Input Block (Option 030)
- MATE (CIIL) Block (Option 700)
- Oven Oscillator Module (Option 010)
- A2 Front Panel Board


## 8-80. Executive Block Assembly

8-81. The Executive Block controls the overall operation of the HP 5334B. This MCU receives instructions through the front panel or the HP-IB MCU. The Executive MCU continuously scans the keyboard for any change and updates the display accordingly.

## 8-82. Measurement Block Assembly

8-83. The Measurement Block carries out all measurement functions of the HP 5334B under control of the Measurement MCU. This MCU receives instructions from the Executive MCU and, in turn, controls all functional blocks which input a signal to the Measurement Block.

## 8-84. Input Amplifier Block Assembly

8-85. The Input Amplifier Block contains a pair of matched 100 MHz amplifier circuits, Channel A and Channel B. This circuitry buffers and shapes the input signal before sending it to the Measurement Block.

## 8-86. DAC Block Assembly

8-87. The DAC Block converts a digital code from the Measurement MCU to an analog DC voltage for sctting the amplifier sensitivity and trigger level, or for providing a reference for reading input lcvels and amplitude peaks.

## 8-88. Time Base Block Assembly

$8-89$. The Time Base Block provides a buffered 10 MHz reference signal to the Measurement Block. The 10 MHz is generated by either the standard crystal oscillator circuit on the A1 Main Board or the Option 010 Oven Oscillator. In addition, the Counter will accept an external 10 MHz signal through a rear pancl BNC connector.

## 8-90. HP-IB Block Assembly

8-91. The HP-IB (Hewlett-Packard Interface Bus) Block handles all HP-IB interfacing. The HP-IB MCU decodes commands to the Executive MCU and formats data which is transmitted via this interface.

## 8-92. Power Supply Block Assembly

8-93. The Power Supply Block provides four regulated DC voltages and one unregulated DC voltage for distribution throughout the instrument.

## 8-94. Channel C Input Block Assembly (Option 030)

8-95. The Option 030 Channel C Block allows the Counter to measure frequencies up to 1.3 GHz . Channel C divides the input frequency by a factor of 64 to bring it within the counting range of the Measurement Block.

## 8-96. MATE (CIIL) Block Assembly (Option 700)

8-97. The Option 700 Modular Automatic Test Equipment (MATE) Block contains a microprocessor, program and data memory, buffer space, and decoding logic circuits, that allows the Counter to operate in MATE systems. The MATE circuit gives the Counter the internal capability to process CIIL (Control Interface Intermediate Language) commands. The CIIL commands consist of ASCII characters and are communicated over the Hewlett-Packard Interface Bus (HP-IB).

## 8-98. Oven Oscillator Module (Option 010)

$8-99$. The Option 010 Oven Oscillator is an extremely stable, compact, low-power source of 10 MHz . This option provides the HP 5334B with a high stability timebase. The crystal, along with its associated circuits are all mounted inside a thermally insulated housing.

## 8-100. A2 Front Panel Board Assembly

8-101. The A2 Front Panel Board provides front panel push-button control of all counter functions and displays measurement results, diagnostic information, and failure codes.

## 8-102. DETAILED THEORY OF OPERATION

8 -103. The detailed theory of operation is provided in the following paragraphs. Each assembly theory refers to its associated schematic diagram located at the end of this section.

## 8-104. INPUT AMPLIFIER BLOCK

8 -105. The Input Amplifier block contains a pair of matched 100 MHz amplifier circuits, Channel A and Channel B. These circuits receive input signals through the front panel connectors or the Option 060 rear panel connectors. The input signals are buffered and shaped before going directly to the Multiple-Register Counter
(MRC) in the Measurement block.
8-106. Each input channel has four stages:

- Signal Conditioning
- High and Low Frequency Amplifier
- Schmitt Trigger
- Buffer

8-107. The Input Amplifier block also contains a Relay Driver through which the Measurement MCU controls the relays in the signal conditioning stages. Channels A and B are identical except for a 100 kHz filter in Channel A only, and the switching circuitry for the Separate/Common modes. The following detailed description refers to Channel A but can be applied as well to Channel B.

## 8-108. Input Amplifier Block Circuit Description (Channel A)

8-109. SIGNAL CONDITIONING STAGE. The first stage, Signal Conditioning has the relay switches for setting AC/DC coupling, $50 \Omega / 1 \mathrm{M} \Omega$ Impedance, $\mathrm{X} 1 / \mathrm{X} 10$ Attenuation, Common A/Separate signal path, and Channel A 100 kHz Filter on/off selection. The relays are driven by TTL driver U37, either directly or through inverter U38. The driver receives instructions from the Measurement MCU over the Measurement Data Bus, and sets the signal conditioning parameters according to the front panel setup or HP-IB commands.

8-110. Immediately after the Channel A input connector, relay K 5 selects either straight-through DC coupling or AC coupling through capacitor C95. Relay K6, when closed, provides the $50 \Omega$ input impedance via parallel 100 ohm resistors R120 and R121. The combination of these resistors and C95 forms a 200 kHz High-Pass filter.

8-111. When K6 is open, the input impedance equals 1 Megohm. Input impedance is set by two different combinations of resistors, depending on which input attenuation is being used. In the X1 attenuation setting, the $1 \mathrm{M} \Omega$ impedance is set by series resistors R108, R109, R110, and R95. In the X10 attenuation setting, the impedance is set by resistors R116 and R93. A constant 1 Megohm load is presented to the input signal regardless of the attenuator setting.
$8-112$. The attenuation function is set by relay K 1 . In the X 1 attenuation setting, K 1 shorts out resistor R116. In the X10 attenuation setting, R93 is placed in parallel with R108, R109, R110, and R95. This parallel combination forms a voltage-divider with R116 so that the signal level after R116 equals $10 \%$ of the input amplitude. Variable capacitor C 87 provides frequency compensation for any stray capacitance after the divider.

8-113. The series resistors after the attenuator relay perform other functions in addition to the ones described. R108 provides high frequency line matching and transient input protection. R109 and clamping diodes CR28 and CR29 provide over-voltage protection to the following stage. To reduce distortion from high amplitude signals, R109, R110, and R95 form a voltage-divider such that the signal level after R109 equals approximately $76 \%$ of the signal before R109. This prevents Q6 and Q10 from going into saturation with a 5 V peak-to-peak (p-p) input signal. Capacitor C88 compensates the divider.
$8-114$. The Channel A filter function is set by relay K 2 . When the Filter mode is off, K 2 is closed, bypassing resistor R94. With the Filter mode switched on, K2 is open and the combination of R94 with the shunt capacitance of the Q8 FET gate-source line of -5.2 V forms the 100 kHz Low-Pass filter.

8-115. The last signal conditioning function is the Separate/Common A switching between the two input channels. The Separate or Common signal paths are set by relays K7 and K8. In the Separate mode, K7 is open and K8 is closed, and each channel is connected to its own input connector. In the Common A mode, K7 is closed and K8 is open, so the Channel B circuit after K8 is connected to the Channel A input.

8-116. HIGH AND LOW FREQUENCY AMPLIFIER STAGE. The High and Low frequency amplifier stage consists of parallel high and low frequency buffering circuits. The high frequency path contains an impedance converter circuit with an AC gain of approximately 0.9 ; the bandwidth of the circuit is from approximately 100 Hz to greater than 100 MHz . The low frequency path provides DC trigger level control with an AC gain of approximately 0.9 ; the bandwidth of the circuit is from DC to approximately 100 kHz .

8-117. In the high frequency path, the input signal is AC coupled, via C74, to the FET Q8 gate. Q8 converts the high impedance at the circuit input to a low impedance at the FET source. Resistor R78 biases the FET to saturation and resistor R77 is a buffer to prevent Q 10 from oscillating. Additional current is provided via pull-up resistor R60 to speed-up the positive voltage swings at the FET source with instantaneous trigger level voltage changes. Resistor R76 sinks current from emitter-follower Q10. The signal from the output of Q10 is fed through the low frequency circuit and input back to the base of Q10.

8-118. In the low frequency path, operational amplifier U30, transistors Q6 and Q10 operate together as a differential feedback amplifier. The signal is DC coupled to the op-amp (U30) input at pin 2. A voltage from either the Digital-to-Analog (DAC) Block or the front panel trigger level control goes to the op-amp at pin 3.
Capacitor C79 provides external frequency compensation. On the trigger level control voltage line, R112 and C84 form a low-pass filter to keep out digital noise from the DAC Block. At the output of U30, resistor R79 limits the base drive to transistors Q6 and combines with R61 and C58 to filter out noise on the -5.2 volt supply line. R61 performs the additional function of stabilizing Q6 at high temperatures.

8-119. Common-emitter transistor Q6 operates simultaneously as a low frequency amplifier and as a current source for the Q8 FET in the High Frequency circuit. The current to the FET is determined by emitter resistor R59. The inverted signal at the collector of common-emitter Q6 is summed with the high frequency signal at the source of Q8 and sent through emitter-follower Q10.
$8-120$. The signal gain of the Low Frequency circuit is determined by the feedback resistor R96 and op-amp input resistors R111, R110, and R95. The values of these resistors are chosen to provide a gain equal to the high frequency gain of approximately 0.9 .

8-121. Resistors R96, R111, R110, and R95 also determine the 1.8 V dc gain for the trigger level control voltage. This control voltage from the DAC Block or the Front Panel Control is variable from -2.5 volts to +2.5 volts. The corresponding level shift at the emitter of Q10 ranges from -4 to +4 volts. This level shift is used to cancel out any dc component of the input signal.

8-122. It should be noted that the trigger level control voltage to the Low Frequency circuit does not equal the trigger level voltage range of the instrument. The trigger level range of the HP 5334B is approximately twice the voltage setting of DAC Block or Front Panel Control. This higher range is due to the attenuation in the Signal Conditioning stage and the dc gain in Low Frequency circuit.

8-123. SCHMITT STAGE. The Schmitt stage receives the analog signal from the High and Low Frequency amplifier and converts it to a square wave output. It also provides variable control of the Counter's sensitivity.

8-124. The major component in this circuit is high speed comparator U22A. At the comparator input, resistors R55 and R75 form a .74 X divider to keep the input voltage within a range of -3 to +3 volts. Capacitor C70 provides frequency compensation for this divider. The comparator offset adjustment is set by trimmer potentiometer R58, and resistors R56 and R57. The adjustment range is -20 to +20 millivolts around the zero volt trigger point.

8-125. It should be noted that the Schmitt stage always triggers at zero volts. Setting the Counter's trigger level control does not change the trigger point of the Schmitt. The trigger level control along with the High-Low Frequency amplifier stage compensates for the de level of the input signal and shifts it to zero volts.

8 -126. The input hysteresis is controlled through the comparator's Latch Enable line at pin 4 . The control voltage from the DAC Block or Front Panel Control has a range of approximately -50 to +50 millivolts dc to U22. This result is in an input sensitivity range of approximately 8 millivolts rms to greater than 120 millivolts rms.

8-127. In the Sensitivity Mode, the voltage at the Latch Enable pin is varied through the Front Panel Control thereby affecting the sensitivity of the Counter. The trigger level is automatically set to zero volts.

8 -128. In the Trigger Level Mode, the voltage at the Latch Enable pin is automatically set to approximately +50 millivolts to give maximum sensitivity while the Front Panel Control or the DAC block sets the trigger level.

8-129. The comparator's complementary ECL outputs are buffered by resistors R36E and R36F before the Buffer stage. Resistor pack R37 provides a current sink for the output lines to the -5.2 volt supply.

8-130. BUFFER STAGE. The Buffer stage translates the ECL signals from the Schmitt stage to the appropriate levels for driving the MRC input and the front panel trigger light.

8-131. The major component in the buffer is quad ECL-to-TTL translator U21. In Channel A, U21C drives the MRC input, and U21B is used as a bidirectional one-shot to drive the front panel trigger light through U24E.

8 -132. The driver U21C receives the complementary ECL signals from the Schmitt stage and outputs a single TTL signal. The resistor divider formed by R51 and R52, together with compensation capacitor C54, converts the TTL output to an EECL signal riding on a dc level of approximately +3 volts for input to the MRC.

8-133. The trigger light one-shot driver U21B receives an ECL input signal from one of the Schmitt stage outputs. A reference voltage feeds into the other input from the U21 Vbb line, pin 1, via resistor R53. A positive feedback loop through C47 and R54 triggers the one-shot at a 10 Hz rate. This output goes to TTL buffer U24E, which then drives the front panel trigger light.

## 8-134. DIGITAL-TO-ANALOG CONVERTER (DAC) BLOCK

8-135. The Digital-to-Analog (DAC) Block converts an 8-bit microcomputer (MCU) code to an analog voltage to program the input amplifier trigger level or sensitivity setting. It also provides a dc reference voltage for the READ LEVELS-Trigger levels and READ LEVELS-Peak Levels functions. The DAC Block is controlled by the Measurement MCU.

8-136. The DAC Block contains two identical circuits, DAC A and DAC B. The Measurement MCU sends data to both DAC circuits over the 8 -line Measurement Data Bus. Additionally, there are nine other signals from the Measurement MCU for control of different functions of the DAC Block.

8-137. Each DAC has two parts: A voltage section that performs the digital-to-analog conversion; and a switching section that passes the analog voltage to the appropriate circuit in the Input Amplifier Block, according to the measurement function. Since the two DAC circuits are identical, the following detailed description will refer only to the DAC A circuit but can be applied as well to the DAC B circuit.

## 8-138. DAC Block Circuit Description (DAC A)

8-139. VOLTAGE SELECTION SECTION. The first half of the DAC circuit, the voltage section, contains a DAC Integrated Circuit (IC), two operational amplifiers (op-amps) feedback loops, and an analog CMOS switch. The DAC IC, U33, outputs a current dependent upon the 8 -bit code input from the Measurement MCU. This current is converted into a nonpositive voltage by the first op-amp U25A. Polarity switch U26B and op-amp U25D operate together to convert this nonpositive output to either a positive or negative level.

8-140. The core of this section is DAC U33. This CMOS IC receives an 8 -bit data code from the Measurement MCU at pins 4 through 11 over the Measurement Data Bus. Since this data bus is used for communicating with many other devices, the DAC must be strobed by the MCU at the CHIP SELECT line, pin 12, and the WRITE line at pin 13. These lines latch the valid 8 -bit code into U33 when they both momentarily go low.

8-141. DAC U33 receives an input current at the VREF line, pin 15. The DAC has 8 CMOS switches to route the input current through an internal resistor ladder network either to ground at pin 2 or to the output at pin 1 . The output current is dependent upon the binary code input to the 8 switches. With all data lines latched HIGH, the current at pin 1 is equal to the input current at pin 15; with the data lines latched LOW, all input current is shunted to ground at pin 2 . There are 256 incremental steps of signal level that can appear at the output proportional to the binary weighted input code.

8-142. Op-amp U25A operates in a feedback configuration to act as a current-to-voltage converter. This feedback loop keeps the output voltage of the DAC at zero volts. Schottky diode CR23 protects the DAC output
from negative voltages during circuit power-up which would damage U33. Capacitor C90 compensates the opamp. The input offset nulling for the op-amp loop is determined by resistors R67, R68, and R86. This divider circuit provides $\pm 10 \mathrm{mV}$ of offset adjustment.

8 -143. Potentiometer R102 sets the gain for the current-to-voltage converter loop by adjusting the current supplied to DAC U33 at pin 15 from U35, the 2.5 volt reference IC.

8 -144. The voltage level at the output of U25A is always negative as a result of the signal inversion by U25A opamp. The analog CMOS switch U26B and op-amp U25D work together to convert this nonpositive voltage to either a positive or negative level. The state of the output TTL voltage at U26B pin 10 decides the polarity of the output of the signal at U25D pin 14. The TTL voltage comes from the Measurement MCU. When this line is at a TTL HIGH, the U26B switch closes the contacts between pins 1 and 15, and the output of U25A appears at the output of U25D unaltered. In this case, U25D is acting as a noninverting buffer with resistors R69 and R70 setting a gain of unity or 1 .

8 -145. When the Measurement MCU sends a TTL LOW to the CMOS switch, the contacts close between pins 2 and 15, and the input of U25D pin 12 is set to zero volts by its connection to U33 pin 1. The op-amp U25D inverts the negative voltage from U25A resulting in a positive voltage with a gain of 1 at U25D pin 14.
$8-146$. The reference voltage input to the DAC is +2.5 volts. The output of the current-to-voltage converter, U25A, ranges from zero to -2.5 volts. Since the 8-bit DAC has the potential for 256 current increments, the voltage resolution of the DAC circuit is approximately 10 mV . Because of the scaling that takes place in the Input Amplifier Block (X2), the DAC resolution for the trigger level of the instrument is 20 mV . The output voltage of the buffer U25D ranges from -2.5 to +2.5 volts. The trigger level voltages of the HP 5334B has a range of -5.1 to +5.1 volts. The dc voltages from the DAC block are amplified in the Low Frequency op-amp loop of the Input Amplifier Block. The Measurement MCU can instruct the DAC to output either a steady dc voltage for setting trigger levels, or a rapidly shifting dc voltage for reading the peaks and levels of signals input to Channe A.

8-147. SWITCHING SECTION. The second half of the DAC circuit, the DAC switching section, contains three analog CMOS switches and a comparator. The DAC or Front Panel Control Switch, U26A, passes the dc voltage from either the DAC or the Front Panel Control to the Trigger Level Control Switch, U27C, and the Sensitivity Control Switch, U28C. These switches then direct the voltage to the appropriate circuit in the Input Amplifier Block as required by the selected measurement function. The Trigger Level Control Switch also works with the Read Levels Comparator, U36B, to compare the DAC voltage with the Front Panel Control voltage when operating in the READ LEVELS-Trigger levels mode. All three CMOS switches are controlled by the Measurement MCU.

8-148. The Measurement MCU determines which control voltage will be sent on to the following switches from U26A. The Measurement MCU selects the voltage via the switch control line at pin 11. A TTL LOW from the MCU connects the Front Panel Control voltage from U26A pin 12 to pin 14. A TTL HIGH connects the DAC voltage from U26A pin 13 to pin 14.

8-149. The Trigger Level Control Switch, U27C, selects the type of trigger level control voltage for the Channel A Input Amplifier. A TTL HIGH from the Measurement MCU at U27C pin 9 sets the trigger level for the instrument to 0 volts by connecting the trigger level control line (pin 4) to ground at pin 3. A TTL LOW at pin 9 connects the DAC voltage or the Front Panel Control voltage from U26A to the trigger level control line via pin 5 .

8-150. The Sensitivity Control Switch, U28C, selects the type of sensitivity level control voltage for Channel A Input Amplifier. A TTL HIGH from the Measurement MCU at U28C pin 9 connects the voltage from either the DAC or the Front Panel from U26A to the sensitivity control line via U28C pin 3. A TTL LOW at pin 9 closes the contacts between pins 5 and 4 . This sets the sensitivity level to the Input Amplifier Schmitt stage to ap-
proximately +50 mV . The U22A comparator then sets the sensitivity for the instrument to approximately 8 mV rms sine wave.

8-151. When the Counter is operating normally, switches U26, U27, and U28 are used to select the proper trigger level or hysteresis voltage for the Input Amplifier. If the Counter is in the Trigger Level mode, the amplifier is set to the predetermined sensitivity level and the Front Panel Control or a recalled voltage level from the DAC sets the amplifier trigger level. This allows the user to adjust the trigger level for small signals with dc offset. When the counter is in the Sensitivity mode, the amplifier trigger level is preset to 0 volts and the Front Panel Control or a recalled voltage level from the DAC sets the hysteresis of the Input Amplifier.

8-152. The one area where the DAC B circuitry differs from the DAC A circuitry is following the Trigger Level Control Switch. DAC B has an extra analog switch, U28D. The operation is identical to the other switches such as U27C. During the READ LEVELS-Trigger Levels mode, a TTL HIGH at U28D pin 11 closes the contacts between pins 13 and 14. The Front Panel Control voltage is then present at pin 3 of comparator U36A.

8-153. The DAC operates in three modes. The first mode is the READ LEVELS- Trigger Levels mode. In this mode, the voltage setting of the Front Panel Control is determined by using the Measurement MCU, the DAC, and the comparator U36B. To discover the Front Panel Control setting, the MCU executes binary search, stepping the DAC voltage through its range and monitoring the output of the comparator. As the comparator output toggles, the MCU responds by shifting the DAC voltage closer to the Front Panel Control setting. At the end of the search routine, the DAC voltage is equal to the Front Panel Control setting and this value is sent to the Executive MCU to be displayed.

8-154. The second mode is READ LEVELS-Peak Levels. In this case, the Input Amplifier is used as the comparator instead of U36B. The DAC voltage is directed to the amplifier (at U30 pin 3) to be used as a trigger level control. During the DAC binary search the comparator U22A triggers on the positive and negative peaks of the input waveform, and the trigger points are sensed by the Measurement MCU and displayed as the voltage peaks of the input signal. This method is used when Auto Trigger is enabled and for Pulse Width, and Rise/Fall measurements as well.

8-155. In Auto Trigger, the DAC voltage is first used for performing the READS LEVELS-Peak Levels operation. The Measurement MCU then sets the Counter trigger level by setting the DAC voltage to the $50 \%$ point between the peaks. A Rise/Fall time measurement is similar except that the MCU set the trigger points to the $10 \%$ and $90 \%$ points of the peak values.

8-156. The third mode of DAC operation is to program the amplifier trigger level or the sensitivity that has been stored in CMOS RAM or programmed through HP-IB. The instrument powers up in the Trigger Level mode and enables front panel control of the trigger level or the sensitivity level. Under HP-IB control, the DAC is active and the Front Panel Control is disabled.

## 8-157. EXECUTIVE BLOCK

8-158. Overall operation of the HP 5334B is controlled by the Executive Microcomputer (MCU). It receives instructions from the front panel keyboard or the HP-IB MCU, then sends instructions to and receives data from the Measurement MCU. The Executive MCU continuously scans the keyboard for any change and updates the display annunciators and front panel key lamps accordingly. When a measurement is complete, the Executive MCU accepts the data from the Measurement MCU, then sends the measurement data to the front panel display and the HP-IB MCU.

8-159. The Executive Block contains three major components: The Executive MCU (U19), a 4-to-16 line demultiplexer (U32), and a 4 MHz oscillator (U18).

8-160. The Executive MCU has four 8-bit I/O ports, for a total of $32 \mathrm{I} / \mathrm{O}$ lines. Eight lines are used to communicate over the Executive Data Bus. Another 8 lines are used for communications via the Measurement Data Bus. The remaining 16 lines are used for addressing, controlling, and monitoring functions.

8-161. The 8-bit Executive Data Bus connects the Executive MCU to the HP-IB MCU (U17), and the front panel display drivers (U1 and U2) on the A2 board. The second 8-bit bus, the Measurement Data Bus, connects the Executive MCU to the Measurement MCU (U29) which controls the Measurement Block and the input signal conditioning.

## 8-162. Executive Block Circuit Description

8-163. The Executive MCU (U19) continuously strobes the keyboard through the demultiplexer (U32) with the ABCD address lines. At the same time, it scans the keyboard directly over the Y0 to Y3 lines. The Executive MCU sends a 4-bit binary code sequence over the ABCD lines to the demultiplexer. The binary sequence continuously cycles through 9 of 16 possible combinations. The MCU (U19) is programmed to skip over the unneeded codes.

8-164. The 4-to-16-line demultiplexer decodes each 4-bit code in the binary sequence. The two ENABLE inputs of the demultiplexer are maintained in the logical "0" state so data is continuously accepted. The information is then transmitted to the selected output as determined by the 4 -line ( $A B C D$ ) input address. As the $A B C D$ lines cycle through the sequence, each output line ( X 0 to X 8 ) goes LOW in turn.

8 -165. The first nine output lines of the demultiplexer ( 0 X to X 8 ) go to the front panel keyboard, where they form a 9 -by-4 matrix with the Y0 to Y3 lines. When a key is pressed, one of the strobe lines (X0 to X8) is shorted to one of the scan lines (Y0 to Y3). The MCU (U19) determines the key that was pressed by detecting which strobe line and which scan line went LOW simultaneously.

8-166. The two additional output lines from the demultiplexer (X12 and X14) control the Measurement MCU (U29). Line X12 is connected to the INTERRUPT REQUEST line and X14 is connected to the RESET line. When activated externally, the Executive MCU uses X14 to reset the Measurement MCU and begin program execution, e.g., when the RESET key is pressed, or when power is applied to the instrument. The interrupt request line (X12) is used to initiate a data transfer from the Executive MCU to the Measurement MCU.

8-167. After the Executive MCU interprets and decodes instructions from the front panel keyboard or the HPIB MCU, it sends the appropriate instruction code to the Measurement MCU. In turn, the Measurement MCU programs the Measurement Block, configures the Input Amplifiers as instructed, and makes a measurement.

8-168. When a measurement is complete, the Measurement MCU sends the result over the Measurement Data Bus to the Executive MCU. The measurement data is interpreted and formatted by the Executive MCU, then sent over the Executive Data Bus to the front panel display and the HP-IB MCU.

8 -169. The $4-\mathrm{MHz}$ clock oscillator (U18) provides the clock signal for all three MCUs in the HP 5334B. The 4 MHz output frequency is determined by quartz crystal Y2. The clock signal goes to the XTAL2 line (pin 2) of each microcomputer.

## 8-170. MEASUREMENT BLOCK

8-171. All HP 5334B measurement functions and data manipulation are performed in the Measurement Block under the control of the Measurement Microcomputer (MCU) which receives its instructions from the Executive MCU.

8-172. The Measurement Block has four major components: The Measurement MCU, the Multiple-Register Counter (MRC), the Multi-Function Chip (MFC), and the Interpolator Counters.

8-173. Inputs to this block are from the Input Amplifier, Digital-to-Analog Converter (DAC), Channel C, and Time Base blocks.

## 8-174. Measurement Block Circuit Description

8-175. The overall measurement cycle is controlled by the Measurement MCU (U29). In addition to the components in the Measurement Block, it controls the DAC, and Channel C blocks. Also, in the Input Amplifier Block, the Measurement MCU sets threshold voltages through the DAC Block and sets operator-selected parameters through the Relay Driver (U37).

8-176. The operation of the measurement cycle centers on the continuous interaction between Measurement MCU U29, MRC U20, and MFC U14. The MRC is a programmable Large-System Integration (LSI) counter-on-a-chip containing the registers that accumulate the input measurement data. The MFC is an LSI device that performs various interface functions between the MRC and input/output devices.

8-177. The last part of the block, the Interpolator Counter section, works with the MRC and the MFC to measure the inherent error factor generated in the normal measurement routine, using an analog interpolation technique. The data it sends to the Measurement MCU is used to improve the accuracy of the measurement.

8-178. The Measurement MCU implements the input signal conditioning and front panel setup as instructed by the Executive MCU, and then initiates the measurement cycle by sending instructions to the MRC U20. Instruction data including measurement mode, selection of input, slope, gate timing, and means of arming are written into the MRC control register through the 4-line I/O data bus port (D0 to D3). Data is transferred to and from the MRC over the Measurement Data Bus, and controlled by the CHIP SELECT (CS), READ/WRITE (R/W), and STROBE (STR) lines from the Measurement MCU.

8-179. The Measurement MCU has four 8-bit I/O ports, for a total of $32 \mathrm{I} / \mathrm{O}$ lines. Eight lines are used to send and receive data over the Measurement Data Bus. The other 24 lines are control lines associated with the Counter's functions.

8-180. The Multiple-Register Counter (MRC) contains four registers. The CONTROL register sets up the measurement mode of the MRC and resets the counting registers, synchronizers, and overflow flags as directed by the Measurement MCU. The EVENT register counts pulses from the input signal, while the TIME register counts the $10-\mathrm{MHz}$ time base pulses used as the reference. The STATUS register contains EVENT and TIME register overflow flags and information on the measurement status.

8-181. The Multi-Function Chip (MFC) contains five functionally independent circuits, four of which are used for MRC interfacing. MFC circuits include a Channel C multiplexer, an Arming multiplexer, two Interpolators, and a Time Base buffer.

8-182. The first of the MFC circuits described is the Arming multiplexer. When External Arming is enabled, the MFC Arming multiplexer accepts an external signal from the front panel ARM input via the ARM input (ARMI) line, U14E pin 9 . The ARMING TRIGGER LEVEL is preset to +1.5 V by voltage-divider resistors R21 and R22, and is input via the ATL line at pin 8 of U14E. An internal comparator level-shifts the signal to an EECL level, and feeds this ARM OUT (ARMO) line directly to the MRC.

8 -183. The second MFC circuit is a time base buffer. This circuit converts the ECL level $10-\mathrm{MHz}$ oscillator signal to the TTL level required to drive the oscillator input, pin 19 (OSCI) of U14B, of the MFC interpolators.

8-184. Finally, MFC U14 has two interpolators circuits (U14B, U14C). These circuits accept the START and STOP Interpolator pulses (STI and SPI) from MRC U20. These pulses, which vary from 100 to 200 nanoseconds, represent the time difference (error factor) between the starting or stopping of the input signal and the nearest 10 MHz clock pulse. To reduce this inherent one-count error by a factor of 200 , the detected error is expanded (200X) to a time length which can be measured by the Counter. Then, using known calibration pulses as references, the actual error can be interpolated and the error effectively cancelled by mathematical modifications to the raw data by Measurement MCU U29.

8-185. Without interpolators, the gate signal during a measurement would normally be synchronous with the main clock (time base). The slight time difference between the actual events of Channel A triggering, and the opening and the closing of the gate, would represent an unrecoverable error factor, limiting the accuracy of the measurement. The start and stop interpolators within the HP 5334B provide a method of determining the amount of time error (for both start and stop events) and adjusting the microprocessor gate time factor to compensate. See Figure 8-5.


Figure 8-5. Interpolator Timing Diagram

8-186. Basically, each short interpolation pulse, from MRC U20, is used to rapidly charge a capacitor via a constant current source. When the pulse ends, the capacitor begins a scaled discharge at about $1 / 200$ th the charge rate. This proportionally expands the interpolator error pulse by a factor of 200X. This integrated waveshape is then squared and used to gate the 10 MHz reference signal through an internal NAND gate. In the end, the MFC outputs two 10 MHz TTL pulse streams with a time length ranging from 20 to 40 microseconds, depending on the time differences between the Start and 10 MHz pulses and the Stop and the 10 MHz pulses. See
Figure 8-6.


Figure 8-6. Expanded Interpolator Error Pulse

8-187. The counters following the Interpolators count the number of pulses in each pulse stream from the MFC. The resulting data is used by the Measurement MCU to increase accuracy of the measurement by adding the start time error and subtracting the stop time error. The Interpolator counters, U12 and U13, are dual 4 -stage ripple counters which are clocked by the falling edge of each incoming pulse. As a result, the count in the counters will proportionally reflect the length of each pulse stream coming from the MFC. The output of the counters is multiplexed and can be read by the Measurement MCU from the Measurement Data Bus.

8-188. Measurement signals are accepted through the three MRC channel inputs (CHA, CHB, and CHC). An external reference oscillator signal is accepted from the HP 5334B 10 MHz time base or an external source through the REF input, and external arming signals are received through the EXT input via the MFC. According to the measurement function, selected MRC inputs are channeled to the EVENT and TIME registers where the input pulses are counted and stored as raw measurement data.

8-189. MRC U20 outputs START and STOP Interpolator pulses to the two MFC interpolator circuits (U14B, U14C); one accepts the START pulse (STI), and the other accepts the STOP (SPI). The phase difference between the measurement and reference signals causes a time delay between the EVENT (E) count and the TIME (T) count. The START pulse represents the time from the opening of the E-gate to the start of the T-count, and the STOP pulse represents the time from the closing of the E-gate to the stop of the T-count. Prior to each measurement, the MRC generates 100 and 200 nanosecond pulses to each interpolator to calibrate the STI and SPI pulses.

8-190. Each interpolator has an $8 \mu \mathrm{~A}$ current source and a 2 mA current sink to charge and discharge an external capacitor. The duration of each STI and SPI pulses between 100 and 200 nanoseconds. The interpolators expand the MRC pulses by a factor of 200 via the capacitors. The expanded 20 to 40 microsecond pulses (STIC and SPIC) are used to gate the 10 MHz time base signal (OSCI) through an internal NAND gate. The resulting 10 MHz TTL pulse streams (STIO and SPIO) from the interpolators are input directly to the START and STOP Interpolator Counters.

8-191. The MRC controls the START and STOP Interpolator Counters by clearing the counters with the event register reset (ERR) line when the MRC is reset. The dual, 4-bit binary counters (U12 and U13) are clocked by the falling edge of each incoming pulse from the MFC. The count accumulated in the STI and SPI counters will proportionally reflect the length of each pulse stream. When directed by the Measurement MCU, quad 2-to-1 multiplexers, U15 and U16, transfer the interpolation data to the Measurement Data Bus. Data transfer is controlled by the SELECT line and the OUTPUT ENABLE line.

8-192. A typical Measurement Block cycle executes by inputting the unknown signal and the Time Base to MRC U20 where they are accumulated, counted, and stored as raw measurement data in the MRC's registers. At the same time, the MRC provides START and STOP Interpolator pulses to MFC U14B/C. These pulses represent the gate error factor caused by the phase difference between the unknown signal and the Time Base reference. Along with the error pulse, the MRC outputs calibration pulses of exactly 100 and 200 nanoseconds.

8-193. Each pulse is expanded and converted to a pulse stream in the MFC and sent to Interpolator Counters U12 and U13. The count data is multiplexed onto the Measurement Data Bus when called for by the Measurement MCU. The MCU uses the error and calibration count to determine the time length of the measurement error.

8-194. When the measurement is complete, the Measurement MCU reads the data from the MRC's registers, and the data from the Interpolator Counters. The MCU then performs the necessary calculations to determine the result for the selected function mode. For example, in a frequency measurement, the MCU adjusts the value for T (the Time Base data) to compensate for the error measured by the Interpolator Counters. The value for E , the unknown frequency count, is then divided by the modified T value to determine the frequency. Likewise, dividing T by E would determine the period of the measurement.

The number of accumulated clock pulses combined with the interpolator adjustments is multiplied by the 10 MHz reference clock period to compute TIME:

$$
\text { TIME }=(T \text { count }+ \text { STI adjustment }- \text { SPI adjustment }) \times(100 \mathrm{~ns})
$$

To determine frequency, the MRC EVENT register count is divided by the computed TIME:

## Frequency $=$ EVENTS/TIME

A period measurement is determined by computing:

## Period $=$ TIME/EVENTS

8-195. The measurement data is then interpreted by the Executive MCU, formatted and sent over the Executive Data Bus to the front panel display and the HP-IB MCU.

## 8-196. TIME BASE BLOCK

8-197. The Time Base Block provides a buffered 10 MHz reference signal against which the unknown signal is measured. The 10 MHz signal is generated by either the standard oscillator circuit on the A1 Main Board or the Option 010 ovenized high stability oscillator. In addition, the Counter accepts an external 10 MHz signal through the rear panel TIME BASE BNC connector. Regardless of the source, the reference signal is buffered before going to the Measurement Block.

## 8-198. Time Base Block Circuit Description

8 -199. The Time Base provides the buffered 10 MHz reference signal for MRC U20, and MFC U14, in the Measurement Block.

8-200. The operation of the Time Base Block centers on the triple differential amplifier U11. Quartz crystal Y1 works with amplifier U11B to generate the standard 10 MHz signal, which is output to U11A through the Internal/External Time Base switch (S1) located on the rear panel of the Counter. Schmitt trigger U11B receives the 10 MHz signal from either the standard, option, or external time base, and outputs a square wave to drive U11C, which buffers the signal going to the Measurement Block.

8-201. The output of U11A also goes to the square wave-to-sine wave converter circuit made up of Q1, Q2, and associated components configured as a differential pair. Current through the pair is set by R14. The output is taken single-ended off the collector of Q2 where the signal is filtered through L1, C16, and R7 for the 10 MHz sine wave. When the rear panel TIME BASE switch is set to INT, this circuit outputs a 10 MHz sine wave through coupling capacitor C 6 to the rear panel BNC connector for use by other instruments as a time base reference. When the Counter is set to EXT, the same connector is used as the input jack for an external 10 MHz source and the signals from the converter and internal 10 MHz circuit are disconnected. The external signal is input directly to Schmitt trigger U11A through current limiting resistor R2 and coupling capacitor C17. Diodes CR11 and CR12 limit the signal amplitude to 1.5 volts peak-to-peak.

8-202. The standard oscillator consists of U11B and quartz crystal Y1. Feedback resistors R12C and R12D bias U11B for oscillation. Capacitors C1 and C5 tune the crystal for series resonance at 10 MHz . Pull-down resistor R10D provides current to the ECL output. Resistor R15 damps the fast ECL transitions to prevent RFI (RadioFrequency Interference). The output signal is ac coupled through C8. Note that this capacitor must be removed if the Option 010 oscillator is installed.

8-203. The standard, option, or external 10 MHz signal is coupled through C17 to U11A which acts as a Schmitt trigger. Resistors R10C, R11C, and R11D bias U11A for approximately 100mv of hysteresis. Resistors R10A and R10B sink current from U11A's complimentary ECL outputs.

8-204. U11C is driven single-ended with input pin 12 biased to Vbb at pin 11. Resistors R11A and R11B provide current to U11C's complimentary outputs and resistors R12A and R12B damp the ECL transitions. The signal is ac coupled through C29 and C30 to provide an ECL signal for the MRC external reference input and the MRC oscillator input.

8-205. For the Option 010 oscillator, the Main Board unregulated +15 volt power supply is input directly to the oven oscillator assembly. The +15 volt supply from the Main Board is regulated by U205 to provide +12 volts to the oscillator circuit. Coupling capacitor C8 must be removed, and coupling capacitor C100 must be added when the Option 010 time base is installed.

## 8-206. HP-IB BLOCK

8-207. The HP-IB Block handles all the HP-IB interfacing between the HP 5334B and an external controller. Commands from the controller are decoded and sent to the Executive MCU, and output data from the Executive MCU is formatted and sent back to the controller.

8-208. The components of the HP-IB Block are the HP-IB Microcomputer (MCU) U17, two transceivers (U6 and U7), and several discrete gates along with associated parts. The HP-IB MCU is programmed to handle all HP-IB interface functions. The three TTL logic Integrated Circuits U8, U9, and U10, are used to speed the detection and response to particular HP-IB control lines. The two transceivers drive the DATA lines and the HANDSHAKE lines. The Service Request (SRQ) status line is controlled by the HP-IB MCU through Q3.

8-209. The HP-IB MCU has four 8-bit I/O ports, for a total of 32 I/O lines. Eight lines are used to communicate over the Executive Data Bus. Another eight lines are used for communication over the HP-IB. The remaining 16 lines are used for controlling and monitoring functions.

8-210. The 8-line Executive Data Bus connects HP-IB MCU U17 to Executive MCU U19, which controls the overall operation of the Counter. The second 8 -line bus, the HP-IB Bus, connects the HP-IB MCU to an external controller for remote operation.

8-211. HP-IB uses a Low-True Logic Convention. A TRUE condition is a TTL LOW and a FALSE condition is a TTL HIGH.

## 8-212. HP-IB Block Circuit Description

8-213. The function of this circuit is to interface between the HP-IB and the Executive MCU. There are several HP-IB functions that require a faster response than the HP-IB MCU can provide. These functions are REMOTE ENABLE (REN), INTERFACE CLEAR (IFC), and ATTENTION (ATN). They are the reasons for most of the discrete components in the HP-IB Block.

8-214. U8 is configured as two latches. The REMOTE ENABLE (REN), INTERFACE CLEAR (IFC) lines are connected to these latch circuits which hold the information until the MCU software can read them. The latches are cleared within 1 ms after they are set.

8-215. U9 and U10 allow the HP 5334B to respond quickly to the ATTENTION (ATN) and INTERFACE CLEAR (IFC) lines since the MCU is too slow to detect the lines directly. When ATN goes TRUE ( 0 volts), the Counter immediately releases control of the HP-IB DATA and HANDSHAKE lines and goes into the acceptor handshake mode whereby it will remove the data and handshake signals from the bus within 200 ns . This is accomplished using the discrete gates of U9 and U10 which set both U6 and U7 to receive. When IFC goes TRUE ( 0 volts), control of the data and handshake lines is relinquished to the external controller as all activity on the HP-IB is halted. Diodes CR6, 7, and 10 provide protection from negative voltage spikes on the IFC, REN, and ATN lines. Diode CR9 protects the SRQ output from going negative.

8-216. TTL voltages from U9 and U10 control the direction of data transfer through U6, an 8-line, 3-state bidirectional transceiver and through U7, a 4-line, 3-state bidirectional transceiver.

8-217. U6 DATA lines are control by the Transmit and Receive (T/R) lines and the Chip Disable (CD) line. A pull-up voltage of +3 V is provided for these lines through CR4 and resistor-package R5.

## 8-218. Power-up RESET Circuit Description

8-219. U292 is a supply voltage supervisor that is used as a RESET controller in the HP 5334B. During powerup U292 tests the supply voltage ( +5 V ) and keeps output pin 5 LOW as long as the supply voltage has not reached +4.8 V . When the supply voltage reaches +4.8 V , pin 5 remains LOW for a minimum of 100 ms , which allows the clock in the HP-IB MCU time to stabilize. After the 100 ms delay, pin 5 of U292 goes HIGH and resets the HP-IB MCU, Measurement MCU, and MATE Microprocessor.

## 8-220. POWER SUPPLY BLOCK

8-221. The Power Supply Block provides six regulated dc voltages for distribution throughout the HP 5334B. An unregulated +15 volts is supplied directly to the Option 010 Oven Oscillator.

8-222. Major components in the power supply are a transformer (T1), two bridge rectifiers (CR202 and CR201), and five voltage regulators (U201 through U205, and U701). All regulators are current limited and have thermal shutdown protection. When the HP 5334B is connected to a power source and set to STANDBY, the regulated +15 volt dc supply and the STANDBY LED are operating.

## 8-223. Power Supply Block Circuit Description

8-224. The transformer isolates the Power Supply Block from the filtering and power selection circuitry and supplies stepped-down ac voltages to the two bridge rectifiers. The voltage to CR201 goes through the front panel POWER switch, S2.

8-225. CR201 supplies voltage to five regulators, U201, U202, U203, U204, and U701. The five regulators supply +5 V DIGITAL, +5 V LINEAR, $+3 \mathrm{~V},-5.2 \mathrm{~V}$, and +5 V MATE voltages, respectively. Rectifier CR202 provides +15 V directly to the optional time base, and through switch S 2 A supplies +12 V to the Counter.

## 8-226. CHANNEL C INPUT BLOCK (OPTION 030)

8-227. The Option 030 Channel C Input Block extends the frequency range of the HP 5334B to 1.3 GHz . The Channel C input circuitry conditions and divides the input signal frequency before sending it to the Measurement Block for counting and final display.

8-228. The input signal is received through the front panel INPUT C connector, then coupled, shaped, levelshifted to an ECL level compatible with the input of MFC U14A in the Measurement Block. The Measurement MCU multiplies the signal (EVENT) count, computes the frequency, and sends the result to the Executive MCU to be displayed.

8-229. The Channel C Input Block consists of five major circuits:

- Signal Conditioning
- Amplifier
- Divider
- Peak Detector
- Threshold Comparator

8-230. Each of the above circuit is described in the following paragraphs.

## 8-231. Channel C Input Block Circuit Description

8-232. SIGNAL CONDITIONING STAGE. The input signal from the front panel INPUT C BNC connector is coupled via capacitor C328. Input from RTIP Cable (Option 060) is coupled via capacitor C327. See schematic diagram, Figure 8-26, for more details on coupling capacitors C327 and C328.

8-233. The Attenuator consists of resistors R321 through R325 and attenuates the input signal by 6 dB so that when diode quad limiter CR303 is conducting, an approximate 50 Ohms input impedance is developed. The 6 dB attenuation also keeps the diodes of CR303 from blowing if a 7 V or greater peak voltage source is connected to the input.

8-234. The Limiter consists of diode quad CR303 that limits the voltage sent to the input of U305 (pin 3), first amplifier of the Amplifier stage. CR303 has two diodes of each polarity in parallel, to provide good limiting (to make sure the input voltage does not exceed U305's maximum input specification) and good power handling of the voltage entering amplifier U305.

8-235. AMPLIFIER STAGE. Amplifier stage consists U305, U304, and U303 and associated components. Pullup resistors R316 and R317 force the output of U305 (pin 1) to +5 V . R316, R310, and R306 are swamping resistors used to limit the gain of the amplifiers at low frequencies. They shunt the output thereby reducing the gain.

8-236. DIVIDER STAGE. U302 divides by 64. The input (pin 1 ) is internally biased and capacitively coupled. R327 is a pull-down resistor. Pin 8 of U302 is the bias point with external decoupling (C305). The output of U302 is 1.6 V peak-to-peak at pin 4. Resistors R305 and R304 decrease this output voltage to the standard ECL amplitude of .8 V p-p. R304 also provides -1.2 V Vbb bias via U 301 pin 11. U301 is a ECL line receiver used as a buffer and line driver to send the divide-by- 64 signal to MRC U20, of the Measurement Block. R302 is a pulldown resistor and R301 establishes a $100 \Omega$ source impedance to match the characteristic impedance of the long trace to U20. R326, located near U20 in the Measurement Block, terminates the trace and provides 2.7 V bias for MRC U20 input.

8-237. PEAK DETECTOR. The purpose of the Peak Detector is to detect when an input signal is present or not present. The input power to pin 1 of U302 is sensed by peak detector CR302. It is coupled in through RC network C310 and R309. This network attenuates low frequencies to compensate for the rolloff in the gain at high frequencies in the Amplifier circuit. Only two of the four diodes in CR302 are used. The diode connected to R309 rectifies the RF (Radio Frequency) to generate a signal corresponding to the peak voltage. The diode connected to R308 generates an equal amplitude but opposite polarity signal, which is used to cancel temperature drift. No RF is applied to this diode. The RF diode is biased by applying 12V to R330. This biases CR304 to about 0.7 V . R315 and R309 establish about . 1 ma current in CR302, which should be at +0.2 V when no RF is applied. The voltage on CR304 and CR302 both drift at the same rate so that the voltage across R315 and hence the bias current is independent of temperature. R329, CR305, R312, and R308 provide a similar bias to the compensation diode in CR302, which should have -0.2 V on it. The two diode signals are summed by R313 and R314 to produce a voltage of within a few millivolts of zero, when no RF is applied or a voltage higher than 5 mV , when RF is applied; then is sent to the input of Threshold Comparator U306 (pin 2).

8-238. THRESHOLD COMPARATOR. Threshold Comparator U306 goes high when sufficient dc is generated from the incoming RF to exceed the threshold established by the voltage-divider formed by Threshold Control, potentiometer R328 and resistor R319. Resistor R318 provides one dB of hysteresis. The output comparator U306 (pin 1) is a open collector. Thus, when no signal is present, it goes LOW and biases pin 4 of U301 (ECL Receiver/Buffer) to -5 V , disabling it, and hence preventing the counter from trying to count noise when insufficient signal is present. When the threshold is exceeded, the comparator output is a high impedance, and R303 biases pin 4 of line receiver U301 to -1.2 V Vbb voltage, thus allowing the Counter to count.

## 8-239. A2 FRONT PANEL BOARD

$8-240$. The Front Panel Block contains the display and keyboard circuitry. The front panel provides push-button control of all counter functions, and displays measurement results and diagnostic information, such as error and failure codes. The front panel circuitry is mounted on the A2 board and communicates with the rest of the Counter through the Executive MCU.

8-241. The keyboard has 34 momentary-contact push-button switches. The keyboard status is continuously monitored through a $9 \times 4$ line matrix with nine strobe lines ( X 0 to X 8 ) from the demultiplexer in the Executive Block, and four scan lines ( Y 0 to Y 3 ) that input directly to the Executive MCU.

## 8-242. A2 Front Panel Board Circuit Description

8-243. FRONT PANEL MONITORING. The Executive MCU outputs a sequence of nine 4-bit binary codes to the demultiplexer. As the Executive MCU outputs each 4-bit code, it forces one of nine strobe lines (X0 to X8) to go LOW. While the strobe line is forced LOW, the Executive MCU then senses each of the four scan lines ( Y 0 to Y 3 ) which are normally HIGH. The MCU then outputs the next 4-bit code in the binary sequence until all strobe lines have been accessed, repeating the process continuously. If a key is pressed, a particular strobe line is shorted to one of the scan lines forcing the scan line to go LOW. The MCU determines which key has been pressed by the combination of strobe and scan lines going LOW at the same time.

8-244. The front panel annunciators, including the display digits and key lamps, are controlled by Executive MCU (except both TRIGGER LEVEL A and B, ARM, GATE, and STANDBY LEDs). The annunicators are driven by two drivers (U1 and U2), which receive data from the Executive MCU over the Executive Data Bus. The eight most significant digits in the mantissa are driven by U 1 , while the remaining digits, annunicators, and key lamps are driven by U2. Data transfer is controlled with the two strobe lines (STR1 and STR2) and MODE selection line.

8-245. DATA TRANSFER. To initiate a measurement cycle, the Executive MCU first pulls STR1 LOW with the MODE line HIGH, then sends a 4-bit control word to driver U1 over the Executive Data Bus. Next, the MODE line is pulled LOW. Then on successive HIGH-to-LOW transitions of the STR1 line, eight bytes of data are automatically sequenced over the Executive Data Bus to eight memory locations in the driver's $8 \times 8$ internal static memory. Further transitions of the STR1 line are ignored and the driver returns to normal display operation until a new control word is transferred. Data is then transferred to driver U 2 in the same manner with the STR2 line controlling the data transfer. After a data transfer, the drivers clear the display, and light the appropriate annunciators and key lamps. The Executive MCU then directs the Measurement MCU to start and compute the corresponding measurement.

## 8-246. MATE (CIIL) BLOCK (OPTION 700)

8-247. The Option 700 MATE Block allows the HP 5334B to respond to an additional control language called Control Interface Intermediate Language (CIIL). The instrument will still respond to its native (HP-IB) programming code, but this would only normally be used for troubleshooting and HP-IB operational verification.

8-248. The MATE Block acts as a link between the HP-IB and the Executive microcomputers (MCUs). The MATE Block operates in one of two modes (CIIL or NATive) determined by the setting of a shorting jumper, J701, in the MATE Block or software commands sent to the MATE Block.

8-249. In the native (NAT) mode, the MATE Block is transparent and the communication between the HP-IB and Executive MCUs is as if the HP 5334B does not include the MATE Block. In the CIIL mode, the MATE Block acts as a translator. CIIL commands sent to the instrument are translated by the MATE Block into commands understood by Executive MCU U19.

8-250. The Option 700 MATE Block contains the following major circuits:

- Clock and Logic Driver
- Address Latch
- Data Buffer
- Read/Write Decode
- Executive and HP-IB Input/Output


## 8-251. MATE (CIIL) Block Circuit Description

8-252. CLOCK AND LOGIC DRIVER. The MATE Block uses the reset circuit in the HP-IB Block (U292 and associated components) and the Clock and Logic Driver integrated circuits, U714E/F, U715C, and U707B/C/F to synchronize the microprocessor and microcomputers. The reset circuit holds the reset line for microprocessor U702 (pin 6) LOW for at least 100 ms after the +5 V supply reaches +4.8 V . This 100 ms delay allows U702 clock to stabilize.

8-253. ADDRESS LATCH. The U702 microprocessor has 16 address lines. Eight lines are dedicated to the address bus and eight are shared with the data bus. The eight least significant bits of the address bus are multiplexed with the eight bit bidirectional data bus to one port of U702. The Address Latch (U703), controlled by U702 Address Strobe (AS) signal (pin 39), is used to demultiplex the address.

8-254. DATA BUFFER. The 8-bit bidirectional transceiver U704 is used for data transfers. The direction of the transfer is determined by U702 R/W signal (pin 38), and the outputs of U704 are enabled by the EDLY(L) output of U715C (pin 8). The use of EDLY(L), a delayed and inverted system clock, assures the outputs of U704 are three-stated during the address portion of the address cycle.

8-255. READ/WRITE DECODE. EPROM U709 has two enable lines, 15 address lines, and eight three-state data lines. When an instruction is executed by U702, the Read/Write Decode logic determines if EPROM U709 is being addressed. If so, the addressed data is placed on the data bus and is read on the falling edge of the system clock. The Read/Write Decode logic consists of, U712A, U714A, U707A, U715A, U714C, U712B, U715B, U714D, U712D, U714B, U712C, and U713.

8-256. U708 is an 8 K byte CMOS static RAM. It has two chip select lines, two enable lines, and 13 address lines. The Read/Write Decode logic determines if the RAM is being addressed and whether a read or write cycle is being executed. During a read from RAM, RAMOE(L) is low and RAMWE(L) is high. Both RAMOE(L) and RAMWE(L) are low during a write to RAM.

8-257. During an I/O port read/write, the Read/Write Decode logic decodes the address lines and the R/W(L) line to determine if the $I / O$ port is being read from or written to.

8-258. EXECUTIVE AND HP-IB I/O. When a read I/O is taking place, the input buffer (U710 or U711) is enabled and the output buffer (U705 or U706) is placed into its high impedance state (OFF). For an write I/O, the input buffer is placed into its OFF state while the output buffer is enabled.

## 8-259. OVEN OSCILLATOR MODULE (OPTION 010)

8-260. The Option 010 Oven Oscillator is an extremely stable, compact, low-power source of 10 MHz . The crystal, along with oscillator, circuit buffer amplifier, and oven control circuits are all mounted inside a thermally insulated housing. A block diagram of the oven oscillator is shown in Figure 8-7.

8-261. The oscillator is divided into three sections with each section contained on a separate printed circuit board. The boards are connected by cable assemblies. The arrangement allows the unit to be easily disassembled and operated in the disassembled state on the service bench. The three sections can be separated into the following subsections:

- Oscillator
- Automatic Gain Control
- Impedance Matching Amplifier
- Voltage References
- Output Buffer Amplifier
- Oven Heater and Controller
- Precision Voltage Reference
- Controller Turn-On Current Limiting Circuit
- Heater Transistor Balance Circuit

8-262. The oscillator is a Colpitts-type crystal oscillator which uses the crystal as the series inductor. The crystal (Y1) is a "third overtone" crystal and is operated at 10 MHz . To keep the circuit from oscillating at the crystal's fundamental, or at a different overtone, the mode suppression network consisting of C5, L2, C6, and L3 appears capacitive only at frequencies between 9 MHz and 10.5 MHz . Below and above this frequency range, the network appears inductive. This does not allow the proper phase shift around the loop and thus suppresses oscillations at all frequencies other than 10 MHz .

8-263. Any reactance in series with the crystal causes a change in frequency. Tuning capacitor C 1 is available from the top of the oscillator outer housing. The change in reactance in C 1 allows the oscillator's frequency to be varied over a $20 \mathrm{~Hz}\left(2 \times 10^{-6}\right)$ range.

8-264. ELECTRONIC FREQUENCY CONTROL (EFC). To allow for a fine tuning control, a varactor (CR1) is added in parallel with the C1 tuning capacitor. The varactor's capacitance depends on the dc voltage applied to it (reverse bias). The EFC voltage range is +5 V to -5 V , giving a fine tuning range of about $1 \mathrm{~Hz}\left(1 \times 10^{-7}\right)$. Since one side of the varactor is tied to a reference ( 6.4 V ), a full +5 V applied to the EFC input will still keep CR1 reversed biased. C2 and C3 keep the EFC current from flowing into the crystal circuit.

8-265. AUTOMATIC GAIN CONTROL (AGC). The Automatic Gain Control circuit consists of emitter-follower Q3 and the peak detector circuit formed by C12, C13, CR4, and CR5. The input to the AGC circuit (and output amplifiers; discussed later) is taken across capacitor C10 and applied to Q3. The signal from Q3 goes to the peak detector which develops a dc voltage to control the crystal current. This negative control voltage forms the lower half of a voltage-divider for the base of Q1 (with R6 and R7) which controls the bias current and gain of Q1, thus controlling the output signal level. The voltage across C10 is proportional to the current through the crystal. As the output of the oscillator changes, the output of the peak detector circuit changes to counteract the oscillator signal change. The result is a stable output signal amplitude.

8-266. By adjusting the AGC voltage with R6, the amplitude for the output (at the base of Q3) can be set. R5 sets the AGC limit when R6 is at its minimum resistance.


8-267. RF OUTPUT IMPEDANCE MATCHING AND OUTPUT BUFFER. The signal for the output amplifiers is taken from the same point as the AGC (across C10). The voltage is buffered by Q5, which is an impedance matching stage. Resistors R14 and R15 set the dc bias level; R14 is bypassed by C14. The signal is then applied to the output buffer stage of Q9. R40 provides a $50 \Omega$ source impedance when transformed by T1. The typical gain of Q9 (base-to-collector) is approximately 2.

8-268. VOLTAGE REFERENCES. Constant current diode CR2 feeds 1 mA to zener diode CR3 providing 6.4 V dc for the EFC varactor reference. R12 and C 15 form a filter to attenuate noise from the zener diode. R13 provides current limiting for Q 4 if the 5.7 V line is shorted.

8-269. Oven Heater and Controller Circuit Descriptions

## NOTE

In the following theory of operation, the term OVEN MASS is used to describe the cast aluminum block in which the crystal and crystal electronics are located.

8-270. The purpose of the oven is to shield the oscillator crystal and electronics from normal ambient temperature changes. The oven controller does this by maintaining a constant oven temperature which is higher than the highest expected ambient temperature. The oven circuit is made up of three main blocks: thermistor, amplifier (controller), and heaters.

8-271. A thermistor (RT1) is secured with epoxy into a hole in the oven mass. U3 is the amplifier, and Q7 and Q8 are the heaters. It is the thermistor that senses the oven mass temperature. The thermistor is in one leg of a bridge circuit consisting of RT1, R18, R19, R20, and R21. When the mass temperature changes slightly, a voltage change occurs across the bridge. Amplifier U3 boosts this voltage change and then uses it to control the current through Q7 and Q8. The current flowing through Q7 and Q8 causes a power dissipation in the form of heat, and it is this heat that warms the oven mass. Therefore, when the mass temperature starts to change, the heaters are biased to adjust their power to cancel the impending temperature change.

8-272. WARM-UP: GENERAL OPERATION. If the oscillator has been off for several hours, the mass thermistor will be at the ambient temperature. Assuming this is below the normal oven operating temperature ( $80^{\circ}$ to $84^{\circ} \mathrm{C}$ ), the resistance of the thermistor RT1 is higher than that of R18 + R20, and therefore the voltage at U3(3) is more positive than at U3(2). This causes the output of U3 to be approximately (Vcc -1.5 V ), supplying base current to Q8 through Q6. A separate circuit limits the collector current of Q8 and is described later.

8-273. As the oven mass warms up, the thermistor's resistance begins to drop, causing the voltage at both U3 inputs to drop (the other U3 input voltage drops because the voltage at the junction of R17 and R18, R19 drops due to the lower RT1 resistance). The voltage at U3(3) decreases at a faster rate than at U3(2) and eventually the U3 inputs are equal when RT1 $=$ R20 + R18. At this time, the oven controller "cuts back" and begins to operate in a linear mode, adjusting the collector current in Q8 (and therefore the power dissipated in Q7 and Q8) to keep the oven precisely at its set temperature.

8-274. The purpose of R17 is mainly to reduce the power dissipated in the thermistor which causes it to selfheat above the oven operating temperature.

8-275. R38 and R39 in parallel provide a means of sensing the heater current. During warm-up, the voltage across the parallel resistors is used in the current limit circuit (described later). During normal linear operation, the junction of R38 and R39 is essentially the feedback point for the oven controller loop.

8-276. Q6 is necessary primarily for the condition when the oscillator has been stored at $-55^{\circ} \mathrm{C}$. Since U 3 (at $-55^{\circ} \mathrm{C}$ ) cannot supply enough base current for $\mathrm{Q} 8, \mathrm{Q} 6$ provides the added current gain required.

8 -277. PRECISION VOLTAGE REFERENCE. U2 is a 10.0 V voltage reference. It provides a stable voltage source for the bridge and U1. A change in the bridge reference voltage changes the voltage across the thermistor and hence, the power it dissipates.

8-278. OVEN CONTROLLER TURN-ON CURRENT LIMITING. The turn-on current limiting circuit consists of U18 and associated components. From an initial turn-on condition, the thermistor senses the oven temperature to be LOW. To correct this situation, U3 attempts to drive heavy amounts of current through the Q7 and Q8 heaters. If allowed to continue this way, excessive current will flow. When Vcc is applied to the oven, U1B forces the voltage across R38 and R39 to equal the voltage at U1B(2) by sinking the base current from Q6. By sensing Vcc, the circuit transforms the heater transistors into what appears to be a fixed heater resistance of 47 Ohms typical.

8-279. HEATER TRANSISTOR BALANCE. Because heater transistors Q7 and Q8 are not equally spaced from the crystal, it is necessary to offset the power dissipation between the two transistors. Amplifier U1A references a voltage-divider across Vcc (R25 and R26) and a second divider (R27 and R28) referenced to the midpoint between the heater transistors. This arrangement allows U1A to control the base current of Q7 to ensure the voltage at the midpoint between the heater transistors is a constant percentage of Vcc ( $\approx 0.57 \times \mathrm{Vcc}$ $\pm 2 \%$ ).

## 8-280. DISASSEMBLY AND REASSEMBLY

8-281. Prior to performing disassembly and reassembly procedures, perform the following:
a. Set POWER ON-STBY switch to STBY position.
b. Remove the power cable from 5334B's LINE socket.

## WARNING

When the cover is removed from the hp 5334b, line Voltages are exposed which are dangerous and may cause SERIOUS INJURY IF TOUCHED. DO NOT REMOVE THE COVERS UNLESS IT IS NECESSARY.

## NOTE

Refer to the exploded view in Figure 6-1 when performing the disassembly and reassembly procedures.

8-283. To remove the cover (MP21, 05334-00021), proceed as follows:
a. On the rear panel of the instrument remove the bumper feet (MP4, 4040-1991), one on each side.
b. Remove the one screw ( $0515-0886$ ) that secures the cover and rear panel.
c. Remove the two screws ( $0515-1132$ ) on both sides of the cover. The right side (viewing the 5334 B from the rear panel) has a handle; therefore, removing these screws will enable removal of the handle)
d. Now, slide the cover off the instrument's chassis.
e. Cover replacement procedures are essentially the reverse of the removal procedures.

## 8-284. A1 Main Board Removal and Installation

## 8-285. REMOVAL PROCEDURES. Perform the following:

a. If instrument contains Option 060, remove three "fancy" BNC nuts ( $0590-1251$ ) that secure the INPUT A,B, and C rear panel BNC connectors.
b. On rear of the instrument, remove "fancy" BNC nut ( $0590-1251$ ) that secures TIME BASE IN/OUT BNC connector.
c. Remove two black hex-head screws $(0380-1332)$ and the two split-lock washers $(2190-0577)$ that secure the HP-IB connector.
d. Remove the three screws (0515-0886) that secure rectifier CR201 and voltage regulators U201 through U205, and U701 heat sink to the rear panel.
e. If instrument has Option 010 , remove two long screws ( $2360-0129$ ) on the left side of chassis (viewing from the rear) that secures the oven oscillator, then unplug the oscillator from its connector, J204.
f. Remove four screws (0515-1055), two on each side, that secure the the Front Panel Assemby to the front of chassis.
g. Remove four feet (MP10, 5040-7201) from bottom of the chassis.
h. Now, perform the steps described in paragraphs 8-286 through 8-288, Front Panel Removal.
i. Remove four screws (0515-0886) and lock washers (2190-0586) that secure four spacers (0533420202) and the transformer (T1) to chassis.
j. Remove the chassis. A1 Main Board is now accessible for repairing or troubleshooting.

## 8-286. INSTALLATION PROCEDURES. Install A1 Main Board as follows:

a. Position A1 Main Board into chassis, so that the HP-IB connector, BNC, toggle switch, and 3 tabs are through the rear.
b. Peform the Removal procedures in reverse.

## 8-287. A2 Front Panel Assembly Removal and Installation

8-288. The A2 Front Panel Board is part of the Front Panel Assembly. To remove the A2 board, the Front Panel Assembly must be removed from the chassis first. Then the Front Panel is removed from the Front Frame and the A2 board from the Front Panel.

8-289. REMOVAL PROCEDURE. Remove the A2 board as follows:
a. Remove cover as described under paragraph 8-282.
b. At bottom of instrument, remove two front feet and two screws (0515-0890) in Front Panel Assembly frame.
c. At top front of instrument, snap-off the plastic trim strip (MP11, 5040-7202) with a small flat blade screw driver.
d. Remove two screws (0515-0890) attaching the Front Panel (MP19, 05334-00019 - Standard Front Panel; 05334-00024 Option 030 Front Panel) to the Front Frame (MP23, 05334-20201).
e. Remove two Trigger Level Knobs (MP25, 0370-1005).
f. Remove three "fancy" BNC nuts (0590-1251) that secure the INPUT A, B, and ARM connectors.
g. Now, separate the Front Panel Assembly from the chassis.
h. Unplug A2 Front Panel Board from A1 Main Board.
i. The A2 Board is now accessible.

8-290. INSTALLATION PROCEDURE. To install or replace A2 Front Panel Board, perform the following:
a. Align A2 board with back of Front Panel and snap into place. There are four places to hold the board in place. Insure these are set. Adjust board to center keycaps.
b. Secure the two Trigger Level potentiometers (pots) using one flat washer, lock washer and nut for each pot. Hand start the nuts. Tighten using $5 / 16$ spin-tight.
c. Using a small flat blade screwdriver, set the Trigger Level pots to full counterclockwise positions.
d. Place one knob on one of the pots, aligning the marker with the " $R$ " in ARM on the front panel.
e. Secure the knob by using the proper allen wrench on the set screw. Tighten. Repeat steps $d$ and e for the other pot.
f. Place Front Panel into the Front Frame, pushing up and aligning the BNCs with the front holes and pushing the panel up to get over the Front Frame edge.

8-291. REMOVAL AND INSTALLATION OF FRONT PANEL RED WINDOW. The seven-segment displays can be replaced through the front panel by removing the red window from the panel. To remove the red window, perform the following:
a. To remove the red window (MP24, 05334-40002), place a small flat-blade screwdriver between the window and the front panel along the bottom edge and gently press up and out, then pull out the window.
b. To install the red window, set window into panel, top edge first (make sure the rubber foam gasket, $05334-00011$ is in place), then press down on window gently and snap the bottom edge into place.

## 8-292. TROUBLESHOOTING

8-293. The troubleshooting section is divided into two parts: (1) Signal Tracing and (2) Signature Analysis.
8-294. Other troubleshooting aids are the Operational Verification Tests found in Section IV of this manual. They provide a good place to start the search for a HP 5334B failure. These tests consist of power-up diagnostic checks as well as functional checks of all the Counter circuit blocks.

8-295. For any failure condition, it is suggested that the power supplies be checked first. The next most important signals to check are:
a. The 4 MHz TTL clock for each of the three microcomputers (at pin 2 of A1U17, U19, and U29).
b. The 10 MHz oscillator which the Counter uses for its counting reference (at pin 21 of A1U14 and U20).

8-296. All troubleshooting requires the following preliminary conditions to be met:
a. The Counter must be connected to the proper line power.
b. The line fuse must be good.
c. All power supply voltages must be correct.
d. All printed circuit boards must be correctly installed.
e. The Counter must be clean and dry.
f. The Counter must have been inspected for broken or missing parts.
g. All safety precautions must have been observed.

## CAUTION

The assemblies and components involved in the following troubleshooting sections are static sensitive, and should be handled at a static-free work area, and in accordance with approved procedures.

## 8-297. Electrostatic Discharge (ESD)

8-298. Electronic components and assemblies can be permanently damaged by electrostatic discharge. To avoid ESD, use the following precautions:
a. Ensure that static sensitive devices or assemblies are serviced at static-safe work stations providing proper grounding for service personnel (e.g., wrist straps).
b. Ensure that static sensitive devices or assemblies are stored in static-shielding containers.
c. DO NOT wear clothing subject to static charge build-up, such as wool or synthetic materials.
d. DO NOT handle components or assemblies in carpeted areas.
e. DO NOT remove the circuit from its conductive foam pad until you are ready to install it.
f. Avoid touching component leads, handle by the plastic package only.

## 8-299. Signal Tracing

$8-300$. This method of troubleshooting uses the conventional techniques of measuring signal levels and observing waveforms with a multimeter and oscilloscope. Sometimes a known signal is introduced to the suspect circuit using an external generator, and other times it is the normal operation of the instrument under test that is studied.

8-301. Signal level troubleshooting for each functional part of the HP 5334B is described in the following paragraphs.

## 8-302. POWER SUPPLY TROUBLESHOOTING

8-303. Use basic methods to troubleshoot the power supply. Make voltage and resistance checks with a Digital Multimeter (DMM) and oscilloscope. Measure all regulator and rectifier dc outputs for the correct voltages and check for shorts to ground. Figure 8-24 shows the Power Supply circuits.

8-304. The HP 5334B contains four dc supplies, shown in Tables 8-8 and 8-9.

Table 8-8. Power Supplies Resistance Checks

| RESISTANCE TO GROUND AT RECULATOR OUTPUTS* (POWER OFF) |  |  |
| :---: | :---: | :---: |
| VOLTAGE | TEST POINT | RESISTANCE |
| -5.2V | A1TP3 | 350 Ohms |
| +5.0V DIC. | A1TP4 | 228 Ohms |
| +3.0V | A1TP5 | 85 Ohms |
| +5.0V LIN. | A1TP6 | 589 Ohms |
| +12.0V | A1TP7 | 229 Ohms |
| +5.0V MATE | A1TPX | 489 Ohms |
| * Note that the resistance values listed above are nominal values only and may differ slightly from instrument to instrument. These values should be used only as a possible indication of a problem. |  |  |

Table 8-9. DC Voltages Check

| VOLTAGE | TEST POINT | RESISTANCE |
| :---: | :---: | :---: |
| $-5.20 \mathrm{~V} \pm 0.26 \mathrm{~V}$ | A1TP3 | NONE |
| +5.00 V DIG. $\pm 0.20 \mathrm{~V}$ | A1TP4 | NONE |
| $+3.00 \mathrm{~V} \pm 0.02 \mathrm{~V}$ | A1TP5 | A1R202 |
| +5.00 V LIN. $\pm 0.20 \mathrm{~V}$ | A1TP6 | NONE |
| $+12.00 \mathrm{~V} \pm 1.00 \mathrm{~V}$ | A1TP7 | NONE |
| $+5.00 \mathrm{~V} M A T E \pm 0.20 \mathrm{~V}$ | A1TPX | NONE |

8-305. The ac outputs from the transformer can be measured at connector A1J201. They should be measured only in reference to ground (Yellow secondary winding, pin 4). MEASURE ACROSS THE TRANSFORMER WINDINGS. The voltages shown below should be seen when measuring with an oscilloscope set for a ac input, using a 10:1 probe. Transformer (A1T1) Output Windings measured to ground A1J201 pin 4 (Yellow wire):

Blue measured to ground $=20 \mathrm{~V}$ p-p
Red measured to ground $=20 \mathrm{~V}$ p-p

## 8-306. INPUT AMPLIFIER TROUBLESHOOTING

8-307. Some possible failures in the Input Amplifier are described in the following paragraphs. Note that there are no Failure Messages which apply to this block. A digital voltmeter should be used for all the de voltage checks, and an oscilloscope with a high impedance, low capacitance, 10:1 divider probe should be used for all the ac signal tracing. A variable signal source, such as the HP 3325A Function Generator or its equivalent, can be used to provide the input signals to the Counter.

8-308. Should the instrument fail while in the measurement mode with the display showing only dashes, it may indicate that the Input Amplifier is not passing the input signal to the MRC. Check for an ECL signal of approximately 0.8 V p-p on a dc level of +3 V at the appropriate MRC input (U20, pin 30 for Channel A or U20, pin 28 for Channel B). If the signal is incorrect or missing, troubleshoot the input amplifier.

8-309. This troubleshooting sequence will cover only the Channel A circuit down to the component level since the Channel B circuit is similar.

8-310. Beginning at the input, the possible failures in the signal conditioning stage include sticky relays, defective relay drivers, and burnt-out input impedance resistors.
$8-311$. To check the ac/dc coupling:
Settings of HP 5334B Under Test
Setting of Signal Source
FREQ A
ON
$100 \mathrm{kHz}, 1 \mathrm{~V}$ p-p, Sine Wave
(set HP 3325A AMPTD to .5 V to generate a 1 V p-p signal)

1 volt, dc offset
AC Coupling. OFF
a. Connect input signal to Channel A Input.
b. Measure the ac signal at pin 14 (or the junction of C 95 and C 87 ) of the coupling selector relay K5. It should be equal to the input signal.
c. While monitoring pin 14 , set the Counter to AC coupling (LED ON). The observed signal should now have no dc offset.
$8-312$. If the Coupling function is defective:
a. Check the relay control line at K5, pin 6 (or anode of CR32). When toggling the AC button, the voltage measured should switch from a TTL HIGH level in the AC mode to a TTL LOW level in the DC mode.
b. Measuring the correct voltages at anode of CR32 indicate a defective relay, while incorrect voltages possibly indicate a defective driver (U37) or buffer gate (U38C).

8-313. To check the $50 \Omega / 1 \mathrm{M} \Omega$ IMPEDANCE function:
a. Remove any input from the Counter.
b. Set 5334B to the dc coupling mode and toggle the $50 \Omega$ key. Measure the input resistance at the Channel A Input connector for each setting with a DVM or DMM. (Measure from the BNC connector center pin to Ground.)
c. The $50 \Omega$ impedance should measure to within $\pm 5 \Omega$, and the $1 \mathrm{M} \Omega$ impedance should be correct to within $\pm 10 \mathrm{k} \Omega$.

8-314. If the input resistance does not change as the $50 \Omega$ key is pressed:
a. Check the control voltage at pin 3 of relay K6 (or anode of CR33). The voltage should switch from a TTL HIGH level in the $1 \mathrm{M} \Omega$ mode to a TTL LOW level in the $50 \Omega$ mode.
b. If this line toggles correctly, it indicates that relay K 6 is defective. An incorrect voltage measured here indicates a defective drive output from U37. Should the impedance measurements be out of tolerance, check the appropriate resistors for any shorts or opens.

Resistor Combinations:
$50 \Omega$ - made up of R120 and R121 in parallel.
$1 \mathrm{M} \Omega$ in X1 Attenuation mode - series combination of R108, 109, 110, and 95.
$1 \mathrm{M} \Omega$ in X10 Attenuation mode - series combination of R116 and R93.
$8-315$. The $\mathrm{X} 1 / \mathrm{X} 10$ ATTENUATION function can be checked:
a. Apply a $100 \mathrm{kHz}, 1$ volt peak-to-peak sine wave signal to the Channel A Input.
b. Set the Channel A Input to X1 attenuation (X10 ATTN LED OFF) and $50 \Omega$ input impedance.
c. Measure the ac voltage at the cathode of CR29 where the amplitude should be approximately 700 millivolts p -p.
d. When the Counter is switched to the X10 attenuation setting (AUTO TRIG must be OFF in order to switch to X10 mode), the amplitude should drop to at least one-tenth the original value, i.e., less than or equal to 70 millivolts p -p.

8-316. If the Attenuation function is defective:
a. Check the relay control voltage at pin 6 of relay K 1 (or anode of CR25). As before, the status of the relay control voltages indicates whether the relay or the driver is at fault. The voltage should switch from a TTL HIGH level in the X10 attenuation mode to a TTL LOW level in the X1 attenuation mode.
b. The resistors that determine the attenuation value should be checked for incorrect values, opens, or shorts. Note that resistors R108, 109, 110, and 95 are included in both X1 and X10 attenuation paths.

8-317. The COMMON/SEPARATE A function can be checked:
a. Remove any input signal from the Counter and set the input impedance to $1 \mathrm{M} \Omega$.
b. Measure the resistance across the contacts of relays K7 and K8. In the Separate mode, K7 should be open and K8 should be closed. The resistance between pins 1 and 4 of $K 7$ should be approximately $2 \mathrm{M} \Omega$. In the Common A mode, K7 should be closed, and K8 should be open. In this case, the resistance across K8, pins 1 and 4, should be greater than $10 \mathrm{M} \Omega$. When closed, both relays should measure less than $1 \Omega$ between pins 1 and 4.

8-318. If the Separate/Common A function does not work:
Check the relay control voltage at pin 3 of relay K7 (or anode of CR30) and relay K8 (or anode of CR31). The voltage is a TTL HIGH level when the relay is open and a TTL LOW level when closed.

8-319. The Channel A 100 kHz FILTER function can be checked:
a. Apply a $100 \mathrm{kHz}, 1$ volt peak-to-peak sine wave signal to the Channel A Input with the input impedance set to $50 \Omega$. Note - set HP3325A AMPTD to .5V to generate a 1V p-p signal.
b. Set 5334B INPUT A to DC coupling.
c. With the Filter A function switched OFF, the amplitude at pin 1 of Filter Relay K2 (or R94 and C74 junction) should be approximately 350 millivolts p-p. When Filter A is turned ON , the amplitude drops to approximately 130 millivolts peak-to-peak.

8-320. If the Filter Relay does not work:
a. Check the relay control voltage at pin 3 of relay K 2 (or anode of CR21). The voltage is a TTL LOW level when the Filter A function is OFF and a TTL HIGH level when the filter is selected.
b. Set $100 \mathbf{k H z}$ Filter A to OFF.

8-321. In the HIGH-LOW FREQUENCY AMPLIFIER STAGE, the most likely failure will be one of the four active components in the circuit: Q8, Q10, Q6, and U30. A problem in one frequency path may cause faulty signal voltages in the other. Since the two paths may cause faulty signal voltages in the other, this stage must be checked by tracing both high and low frequency signals through the circuit followed by various dc checks. Note that a $10: 1,10 \mathrm{M} \Omega$ oscilloscope probe must be used at the gate of Q 8 and at the inputs of operational amplifier U 30 to prevent loading down the signal.

8-322. To check the HIGH FREQUENCY path set the equipment as follows:
5334B Signal Source
FREQ A..........................................ON
$1 \mathrm{MHz}, 1$ Volt peak-to-peak sine wave
(set 3325A AMPTD to . 5 V to generate 1 V p-p signal)
0 volt, dc offset
$50 \Omega$ ON
AUTO TRIG. OFF
a. Apply the 1 MHz signal to the Channel A Input.
b. Adjust the TRIGGER LEVEL/SENS control for a 0 volt dc level at the emitter of Q10.
c. Measure approximately 350 millivolts p-p at the emitter of Q10.

8-323. If the high frequency signal is not getting through, trace the signal through the circuit and check the component that is not passing the signal. Remember to use a $10 \mathrm{M} \Omega$ probe at the gate of FET Q8.

Measure approximately 280 millivolts p-p with +0.22 volt dc offset at the gate of Q 8 .
8-324. To check the LOW FREQUENCY path set the equipment as follows:
5334B
Signal Source
FREQ A $\qquad$ ON
$1 \mathrm{kHz}, 1$ Volt $\mathrm{p}-\mathrm{p}$ sine wave
(set HP 3325A to $\mathbf{5 V}$ to generate 1 V p-p signal)
0 volt, dc offset
$50 \Omega$
ON
AUTO TRIG................................OFF
a. Apply the 1 kHz signal to the Channel A Input.
b. Adjust the TRIGGER LEVEL/SENS control for a 0 volt dc level at the emitter of Q10.
c. Measure approximately 350 millivolts p-p at the emitter of Q10.

8 -325. Should the low frequency output be incorrect, trace the signal through the low frequency path to find the faulty component. Remember that signal measurements at the input to U30 should be taken with a 10 megohm probe to ensure an accurate reading.
a. Measurement approximately 140 millivolts p-p with no dc offset at the inputs of U30 (pins 2 and 3 ).
b. Measure approximately 10 millivolts p-p with a -1.7 volt dc offset at the output of U 30 (pin 6).

8-326. If the 5334B miscounts, or displays a reading without a signal being applied to it, the problem may be due to self-oscillation in the low frequency circuit. With no input into the Counter, probe the collector of Q6. If a signal is present, changing operational amplifier U30 may clear up the problem.

8-327. To check the Trigger Level function:

## Settings of the 5334B

AUTO TRIG $\qquad$ OFF
a. Remove any input signal to the Counter.
b. Measure +4 to -4 volts at the emitter of Q10 as the front panel TRIGGER LEVEL/SENS control is varied over its full range.

8-328. If the voltage at Q 10 is incorrect:
a. Check that the voltage at the collector of Q6 has the proper range ( $\pm 4$ volts).
b. Check the inputs to the operational amplifier, U30, at pins 2 and 3 . Both inputs should stay at 0 -volt dc regardless of the front panel TRIGGER LEVEL control setting.

8-329. If the voltage at the collector of Q6 is wrong:
a. Check the voltage from the TRIGGER LEVEL at the junction of resistors R112 and R111 near the input of U30. Measure -2.5 to +2.5 volts as the TRIGGER LEVEL is adjusted.
b. This voltage passes through switching circuitry in the DAC block on its way to the operational amplifier, so the TRIGGER LEVEL control or the DAC block may be at fault.

8-330. If the Q6 collector voltage lacks the proper range, check the gain resistors (R95, R96, R110, and R111) before replacing any active components. An open, or shorted, resistor may be the problem. This could cause the voltage at the collector of Q6 to be nonvariable.

8 -331. If the Q 6 collector voltage is stuck at -5 volts, Q 6 is probably shorted. If the voltage is stuck at 0 -volt, the probable cause is a shorted base-to-emitter junction in the emitter-follower, Q10.
$8-332$. If Q 6 collector voltage is stuck at greater than +4 volts:
Check the voltage across the base-to-emitter junction of Q6. If the correct voltage drop of 0.7 volts is measured, Q6 may be open or not turning ON, or Q8 or Q10 may be shorted out.

8-333. If the Q 6 base-to-emitter voltage is not correct:
a. Check Q6 base drive resistor R79 and stabilizing resistor R61 for opens or shorts.
b. Also check filtering capacitor C58 for a possible short. If these components appear to be good, either Q6 or U30 may be defective.

8-334. The next section of the Channel A circuit, the SCHMITT STAGE, has only one active component, comparator $\mathbf{U} 22$. In most cases, replacing U22 will clear up a failure in this stage.

## NOTE

When signal tracing in this circuit, the ECL signals at the output of U22 will show some ringing unless a short ground lead is used on the oscilloscope probe.

8-335. If the SCHMITT STAGE is suspected of failing, set the equipment as follows:

5334B
Signal Source
FREQ A $\qquad$ ON
$1 \mathrm{MHz}, 1$ Volt p-p sine wave
(set HP 3325A AMPTD to .5V to generate a 1V p-p signal)
0 volt, dc offset
$50 \Omega$. ON
SENS ON
SENS control Fully CW
a. Apply the signal to the Channel A Input.
b. Measure the signal amplitude before and after the divider circuit (R55 and R75) at the input of U22A. Measure the signal at the emitter of Q10 where it should equal 350 millivolts p-p and at U22A input pin 7 where it should equal approximately 250 millivolts.
c. If this amplitude is incorrect, check the divider circuit components R55, R75, and C70.
d. Next measure the complementary ECL outputs of the U22A comparator at pins 1 and 2. Observe a +1 V p-p square wave signal with a -1.25 V dc offset. Any ringing on the signal is probably caused by the length of the ground lead on the oscilloscope probe.

8-336. If the Schmitt outputs are missing or incorrect:
a. Verify that the correct input is present before replacing U22. If only one of the two ECL outputs is incorrect, check the resistor pack, R37, for opens or shorts before replacing U22.

8-337. The Comparator Offset adjustment (AVOS, R58) can be checked using the same setup as in the previous tests:
a. Note the present voltage at U22A pin 8. This voltage is needed so that the offset can be returned to its original value.
b. Vary the Channel A voltage offset resistor (AVOS, R58) over its full range. The voltage at pin 8 should vary from +20 to -20 millivolts.
c. If this voltage is incorrect, check the +5 and -5.2 supply voltages at R58. Also check the divider resistors R56 and R57 as well as R58 for opens or shorts.
d. Remember to reset the voltage at pin 8 to its original value after making this check.

8-338. If the SENS control does not work when the Counter is in the Sensitivity mode:
a. Check the LATCH ENABLE line at pin 4 of U22A. The voltage should vary from approximately +50 to -50 millivolts as the SENS control is adjusted over its full range. If these voltages are incorrect, check the SENS control or the DAC block switching circuitry. If the voltage has the correct range, U22 may be defective.

8-339. In the last part of the Channel A circuit, the BUFFER STAGE, a problem can be partially isolated by observing the failure symptoms of the Counter. During a measurement, the display may be incorrect or missing, or the front panel trigger light may fail to flash. If only one of these failures occur, the fault is probably in the buffer stage. Replacing U21 may fix the problem. However, if both of these symptoms occur together, verify the output of the previous Schmitt stage before troubleshooting the buffer stage.
$8-340$. To check the Buffer Stage:
Settings of 5334B
Settings of Signal Source
FREQ A ON
$1 \mathrm{MHz}, 1$ Volt p-p sine wave (set HP3325A AMPTD to .5V to generate a 1V p-p signal) 0 volt, dc offset

$50 \Omega$.
ON

AUTO TRIG...............................OFF
SENS ON
SENS control Fully CW
a. Apply the signal to the Channel A Input and note the failure symptoms.
b. A display problem is caused by the Level-Shifter, U21C which provides the input to the MultipleRegister Counter (MRC). A defective Trigger Light function is caused by the Trigger Light OneShot, U21B.
c. Measure the output of the level-shifter U21C, at pin 12 . If the 1 MHz , TTL signal is missing or incorrect, verify the input to the level-shifter at pins 10 and 11.
d. If the complementary ECL signals are not present, check the damping and pull-down resistor packs, R36 and R37, for opens or shorts. Verify that the output of the Schmitt Stage is correct.

8-341. If the Level-Shifter is operating correctly:
a. Measure the input to the MRC, U 20 of the Executive/Measurement Block. The 1 MHz signal at pin 30 of U 20 should be an ECL signal of 0.8 Volts p-p riding on a dc level of approximately +2.7 volts.
b. If the signal is missing or is a TTL signal, check the voltage divider components R51, R52, and C54 for opens or shorts. Also check the dc level adjustment divider, R128 and R130.

8-342. The Trigger Light One-Shot circuit should cause the front panel trigger light to flash at a 10 Hz rate, when using the same setup and input as before. If the trigger light is dead:
a. Check the output of the one-shot, U21B. The signal at pin 5 should be a 10 Hz TTL signal. If this output is good, the signal may not be reaching the front panel.
b. Trace the signal through the inverter U24E, the current-limiting resistor pack (R118) and finally, to the front panel LED (DS61).

8-343. If the one-shot output is dead:
a. Measure the input at U21B pin 6 and verify the presence of the 1 MHz , ECL signal of +1 volt p-p offset by -1.3 volts dc. Troubelshoot the Schmitt Stage if this signal is missing.
b. If the input is good, disconnect the 1 MHz input to the Counter and measure the dc reference at U 21 B, pin 7. It should be approximately -1.3 volts. If this voltage is incorrect, check the Vbb reference voltage at pin 1 for an approximate level of $\mathbf{- 1 . 3}$ volts. Also check resistor R53 and capacitor C 45 on the reference voltage line for opens or shorts.

8-344. A trigger light failure may be caused by a defective feedback loop. To check for this:
Settings of 5334B
AUTO TRIG..................................OFF
SENS................................................OFF
No Input Signal to the Counter.
a. Vary the TRIGGER LEVEL control over its range and note whether the Trigger Light turns ON and OFF. If the one-shot will not operate manually, replace U21.
b. If the Trigger Light works correctly in the manual mode, but will not flash at approximately 10 Hz rate during a measurement, then the feedback loop is defective. Check the feedback components R54 and C47 for opens or shorts.

## 8-345. DIGITAL-TO-ANALOG CONVERTER (DAC) TROUBLESHOOTING

8-346. Failure symptoms in the DAC block include not being able to perform the DAC Zero or DAC Gain Adjustments, and a defective READ LEVELS-Trigger Levels or READ LEVELS-Peak Levels display. There are no Failure Messages which apply specifically to the DAC block. However, a defective DAC Integrated Circuit may cause a failure message display related to the Measurement Data Bus.

8-347. The READ LEVELS-Trigger Levels function may display an incorrect voltage or polarity as the Trigger Level control is adjusted over its full range of +5.1 to -5.1 volts. If the display is faulty and both the A and B channel trigger levels exhibit the same symptoms, the fault may be with the Measurement microcomputer (MCU), U29 or Measurement Data Bus (U29, I/O Port 4). Check for enabling pulses from the Measurement MCU.
$8-348$. Set the equipment as follows:

HP5334B Under Test
FREQ A............................................ON
AUTO TRIG................................OFF
SENS...............................................OFF
READ LEVELS...........................Trigger Level Mode
a. Use an oscilloscope to check for strobe pulses from Executive MCU (U29 pin 7) to pin 13 of both DACs U33 and U34 (the WRITE lines). Also, check for strobe pulses from U29 pin 32 to pin 12 of U33 and from U29 pin 30 to pin 12 of U34 (the CHIP SELECT lines). Observe a +5 volt peak-topeak pulse train at each measurement point. If the strobe pulses are missing, U29 may be defective.
b. Check the Measurement Data Bus at the DACs for TTL levels on pins 4 through 11. A bent or broken pin may be the source of the problem.

8-349. From this point on, it is assumed that a failure has been isolated to the DAC A circuit. The following troubleshooting information refers to only DAC A circuit components. The two circuits are similar enough so that the troubleshooting techniques can easily be applied to the DAC B circuit if it fails.

8-350. If the DAC A Zero adjustment will not calibrate, check that the adjustment pot, R67, has the correct $\pm 10$ millivolt range. This voltage can be measured at pin 3 of op-amp U25A. If the voltage is correct but the opamp cannot be adjusted for offset, replace U25. If the adjustment voltage is not correct, check the resistor divider, R68 and R86, at the op-amp input as well as the trimmer potentiometer, R67, for opens, shorts, or incorrect values.

8-351. If the DAC A Gain adjustment will not calibrate, check for the correct reference voltages at U35. The +5 volt Linear supply voltage should be present at pin 1 and +2.5 volts should be present at pin 2 and TP10. If the reference voltage is missing or incorrect, check for a short at capacitor C77 on the reference output line before replacing U35. If the reference voltage is correct, the GAIN potentiometer, R102, should provide an adjustment range of approximately +2.5 to +2.1 volts at pin 15 of DAC U33. If this voltage is incorrect, either R102 or U33 is defective.

8-352. To check the operation of the DAC A circuit, set the equipment as follows:

## Settings of 5334B

FREQ A......................................ON
AUTO TRIG................................OFF
No Input Signal to Counter.
a. Short the inverting input of U25A (pin 2) to the +2.5 volt reference at TP10.
b. Measure approximately -3 volts at the output of the DAC voltage circuit, U25D pin 14.
c. If the DAC voltage is not correct, measure the voltage at the output of the current-to-voltage converter, U25A pin 1 and at the output of the Polarity Switch U26B pin 15. Each pin should measure approximately -3 volts.
d. If the current-to-voltage converter output is incorrect, replace U25. If the Polarity Switch output is incorrect, verify that the control signal from the Measurement MCU at U26 pin 10 is a TTL HIGH level. Also check the feedback resistors, R69 and R70, for opens or shorts before replacing U26.
e. Remove jumper from U25A pin 2 and TP10.

## 3-353. Troubleshooting the DAC Switching Section

8-354. To check Polarity Switch, U26A, set the counter as follows:

## Settings of 5334B

READ LEVELS-Trigger Level mode ("L" appears at extreme right side of display.)
No Input Signal to Counter.
a. Rotate the Trigger Level Control over its full range. The input voltage at U26A pin 12 and 14 should range from +2.5 to -2.5 volts.
b. If the input voltage is incorrect, resistor-pack R119 or the Trigger Level Control may be defective.
c. If the output voltage is incorrect, verify that the control voltage from U29 pin 28 to U26A pin 11 is a TTL LOW. If the control voltage is correct, replace U26.

8-355. To check Trigger Level Switch, U27C, set the counter in the READ LEVELS-Trigger Level mode, with no signal connected to the Counter's input.
a. With the SENS key OFF, the output at U27C pin 4 should range from +2.5 to -2.5 volts as the Trigger Level Control is adjusted.
b. With the SENS key ON, switch output should remain at zero volts, regardless of the Trigger Level Control setting.
c. If the switch is not operating correctly, check for the correct TTL levels at control pin U27C pin 9, before replacing U27. When the SENS key is OFF, the TTL level should be LOW; when the SENS key is ON, the TTL level should be HIGH.

8-356. Check the READ LEVELS comparator, U36B, with no signal connected to the Counter's input.

## Settings of 5334B

AUTO TRIG................................OFF
READ LEVELS............................OFF
SENS........................................... OFF
a. Rotate the Trigger Level Control over its full range. The output of the comparator U36B pin 7 should toggle between +5 and -5 volts as the Trigger Level Control is adjusted through the midrange position.
b. If the output does not toggle, set the Counter to READ LEVELS-Trigger Level mode and check the input pins of the comparator with an oscilloscope. The voltage at U36B pin 5 should vary between $\pm 2.5$ volts as the Trigger Level Control is adjusted. At pin 6, the DAC voltage should be slewing rapidly across its range in a search routine. If both of these inputs are correct, replace U36.

8-357. To check the Sensitivity Control Switch, U28C leave the counter in the READ LEVELS mode, and press the SENS key ON.
a. As the Trigger Level Control is rotated, the output of U28C pin 4 should vary from +40 to -40 millivolts.
b. With the SENS key OFF, the output of the switch should remain at +40 mV , regardless of the Trigger Level Control setting.
c. If the switch does not function correctly, check the TTL levels from U29 pin 27 to the control pin 9 of U28C. With the SENS key ON, the level should be a TTL HIGH; with the SENS key OFF, the level should be a TTL LOW.

## 8-358. MEASUREMENT BLOCK TROUBLESHOOTING

3-359. Use the Failure Messages from Table 3-4, in the Operating and Programming Manual, to help troubleshoot the Measurement Block. The failure codes which indicate problems in the Measurement Block focus primarily on the Measurement microcomputer (MCU) or on communication problems between the MCUs.

3-360. The failure codes 7.0 to 7.5 deal primarily with failures of the Measurement MCU. During power-up, the MCU performs a RAM and ROM check. If it passes the test, the processor alternately flashes the front panel GATE and ARM annunciator lights during the power-up sequence. It then carries out an I/O port check, and also checks the MRC. The processor will also detect the absence of the 10 MHz Time Base signal. All the failure codes in this group are generated solely by the Measurement MCU.

3-361. The 9.X failure codes focus on data communication between MCUs. If the Measurement MCU does not respond correctly, the Executive MCU will generate one of two possible failure codes ( 9.1 or 9.3).

3-362. If no failure codes are generated and the operation of the Measurement MCU is in question, it is possible to test the MCU separately from the rest of the instrument. This is done by placing the MCU into a diagnostic mode using the following instructions.

## Setup

a. Begin with the 5334 B in STANDBY.
b. Connect a jumper between the Measurement MCU (U29) TP12 and Ground (TP8).
c. Apply power to the 5334B and observe that the Counter displays "FAIL 9.1".
d. Remove jumper from TP12 and TP8.

## NOTE

Be careful to place the scope probe on one pin at a time. If two pins are accidently shorted by the scope probe, you may not observe the correct signals. You will have to repeat the steps a through $d$ of the Setup procedure.

Test
a. Use an oscilloscope to observe the signals described below. All are TTL levels

U29 Measurement MCU
Pin $1-4 \mathrm{MHz}$ sawtooth waveform
Pin $2-4 \mathrm{MHz}$ sine wave with no dc offset voltage
Pin 3 - LOW
Pin 4 and Pin 5 - Line Toggles
Pin 6 - HIGH
Pin 7 to Pin 15 - Line Toggles
Pin 16 - HIGH
Pin 17 and Pin 18 - Line Toggles
Pin 19 - HIGH
Pin 20 - LOW
Pin 21 - LOW
Pin 22 to Pin 37 - Line Toggles
Pin 38 - HIGH
Pin 39 - HIGH
Pin 40 - HIGH
b. If any signals measured are incorrect, replace the Measurement MCU (U29).

8-363. If there is still trouble in the Measurement Block, check to see if a RATIO A/B measurement can be performed by connecting the 10 MHz Time Base output from the rear panel to the Channel A Input and setting the COMMON A mode. This ratio measurement uses only the E and T registers in the Multiple-Register Counter (MRC) and not the Interpolators. The measurement should be $1.000000 \pm .000001$.

8-364. If the Counter does not perform the RATIO measurement correctly:
a. Verify that the 10 MHz Time Base signal is getting to the MRC at U20 pin 21. This signal should have a minimum amplitude of 600 millivolts peak-to-peak.
b. Check the Channel A and B inputs to the MRC U20 at pins 28 and 30 . There should be a 10 MHz signal with an amplitude of 800 millivolts on a dc level of +2.4 to +3 volts at both pins. Also check to see that the control lines from the Measurement MCU at pins 1,3, and 40 of U20 are changing state at TTL levels.
c. If all of these signals are observed, yet a RATIO A/B measurement cannot be performed, replace MRC U20.

8-365. If the RATIO measurement is good, set the counter to FREQUENCY A, still using the 10 MHz reference as an input. If the measurement varies more than $\pm 2$ counts, the interpolator circuitry is defective.
a. Check the interpolator output of MRC U20 at pins 13 and 16. The interpolator pulses at these output pins will be too small to measure, but the dc level should be between +2.0 volts and +2.3 volts.
b. Check the Interpolator outputs of the Multi-Function Counter (MFC) U14 at pins 11 and 17 with an oscilloscope. The low frequency pulse streams should be visible with an amplitude of 100 mV riding on a dc level of +4 volts.

## 8-366. EXECUTIVE BLOCK TROUBLESHOOTING

8-367. Failure Messages that can indicate problems in the Executive Block are referred to in Table 3-4, in the Operating and Programming Manual. The two categories of failure are:

- Failure of the Executive microcomputer (MCU)
- Failures in communication between the MCUs

8-368. The first category deals with the the internal ROM and RAM of the Executive MCU which is checked during power-up. The failure codes are 6.0 and 6.1.
$8-369$. The second category covers communication between MCUs. This is checked at power-up and continuously while the Counter is operating. The failure codes are 9.0, 9.3, and 9.4.

8-370. If Failure Messages do not provide the cause of the problem, it is suggested that Signature Analysis be used to troubleshoot the Executive Block. The instructions for using Signature Analysis to troubleshoot the 5334B are listed following the paragraph 8-456, SIGNATURE ANALYSIS.

## 8-371. FRONT PANEL BLOCK TROUBLESHOOTING

8-372. Should the Display and Keyboard Block fail, it is possible to use the power-on diagnostics to isolate the problem. The power-on test lights all front panel LEDs. Refer to the Operational Verification Tests in Section IV of the Operating and Programming Manual for more details.

8-373. The seven-segment displays can be replaced individually. These displays are checked by running through the power-on test or by selecting the GATE TIME and entering a sequence of 8 's on the display. If only one display is not working, replacing it should clear up the problem. If more than one display is faulty, the problem is probably elsewhere in the block. If only the 8 left-most displays or the 2 right-most displays are faulty, the respective driver, U 1 or U 2 , is probably bad. The seven-segment displays can be replaced through the front panel by performing the removal and installation procedures in paragraph 8-291.

8-374. If the entire display is defective, another component sharing the Executive Data Bus may be at fault. Remove the HP-IB microcomputer (MCU) U17 to see if the problem clears up. If not, replace the the Executive MCU (U19). Should the problem still exist, drivers U1 and U2 are probably bad. After front panel disassembly (refer to paragraph 8-287 for procedure to disassemble the front panel), the defective driver can be found by switching U1 with U2. Only one driver at a time should be plugged back in, as the defective one may be shorting the Executive Data Bus.

8-375. Note that there are two sets of codes which the 5334B may display. The first set of codes, called Error Messages, indicate operator errors, either through incorrect keyboard entry or incorrect HP-IB programming. The second set of codes, called Failure Messages, indicate internal hardware failures which may occur in a particular area of the Counter. A complete list of codes is provided in Tables 3-3 and 3-4 of the Operating and Programming Manual.

## 8-376. TIME BASE TROUBLESHOOTING

8-377. There is only one failure mode which applies to the Time Base block. The Measurement microcomputer (MCU) tests for the presence of the Time Base during the power-up sequence and displays a "NO OSC" (no oscillator) message if the signal is missing.

8-378. The time base circuit can be serviced by signal tracing with an oscilloscope that has at least a 50 MHz bandwidth. The components most likely to fail are U11 and the standard oscillator or the Option 010 Oven Oscillator.

8-379. If the STANDARD crystal oscillator, Y1 fails:
a. Power-up the 5334B Counter.
b. Check for a 10 MHz square wave with an amplitude of approximately 100 mV p-p at U11B pin 7.
c. Check for a $1 V$ p-p, 10 MHz square wave at U11A pins 2 and 3, and U11C pins 14 and 15.
d. Check Vbb at pin 11. It should measure +3.8 volts. Note that U11 is powered between ground and +5 volts instead of the customary ground and -5 volts. As a result the ECL output signal rides on an approximate +3.2 dc level.
e. If any outputs are dead, verify that the $1 \mathrm{~K} \Omega$ pull-down resistors are not shorted before replacing U11.
f. Check the Square Wave to Sine Wave Converter for a complementary square wave at the base of both Q1 and Q2. A sine wave should be observed at the collector of Q2. If there is no output, check if L1 is open or if C16 is shorted before replacing Q1 and Q2.

8-380. If Option 010 Oven Oscillator is suspected of a problem:
a. Check for +12 volts across J 204 pins 3 ( +12 OSC SUPPLY) and pin 2 (oscillator circuit common).
b. Check for +15 V unregulated $(\approx+18 \mathrm{~V}$ ) across J 204 pin 14 (oven $(+)$ supply) and pin 15 (oven common).
c. Check at J 204 pin 1 for a 10 MHz sine wave with an amplitude of 2.25 V peak-to-peak.
d. If the correct dc voltage appear at J 204 but no sine wave is present at pin 1, check the oven oscillator unit as described in the following paragraphs.

## 3-381. TROUBLESHOOTING OPTION 010 OVEN OSCILLATOR

## 3-382. Inspection

8-383. The oscillator should be inspected for indications of mechanical and electrical defests. Electronic components that show signs of overheating, leakage, frayed insulation, and other signs of deterioration should be checked and a thorough investigation of the associated circuitry should be made to verify proper operation. Mechanical parts should be inspected for excessive wear, looseness, misalignment, corrosion, and other signs of deterioration.

## 3-384. Special Parts Replacement Considerations

8-385. Refer to schematic diagram Figure 8-27. Several mechanical parts and components must be replaced as a pair or require other special consideration. They are:
a. Oven mass assembly and thermistor: If the thermistor (RT1) is found to be defective, the thermistor and oven mass assembly must be replaced as one item, HP Part Number 10811-60106. Do not attempt to replace the thermistor alone.
b. Crystal and Temperature Set Resistor: The replacement crystal for Y 1 is accompanied by the required temperature set resistor (R20) for the oven. This resistor must be installed with the new crystal. The crystal and R20 can be ordered using HP Part Number 10811-60108. If only the temperature set resistor (R20) is found to be defective, it must be replaced with the same value and tolerance. If the resistor ( R 20 ) is unreadable, the value required can be determined by finding the oven temperature value marked on the crystal (Y1). The required resistor can then be determined from Table $8-10$. When Y 1 is replaced, the nut which secures it to the oven mass should be tightened to a torque of 0.6 newton-meters ( 5 in .-lbs). This insures maximum heat transfer without over-stressing the crystal package.

Table 8-10. Temperature Set Resistor List

| OVEN TEMP ${ }^{\circ} \mathbf{C}$ | RESISTOR VALUE | PART NUMBER |
| :---: | :---: | :---: |
| 80.0 | 1.33 K | $0698-7239$ |
| 84.0 | 0 | $8159-0005$ |

c. Oven heater transistors Q7 and Q8: Holding screws for Q7 and Q8 must also be torqued to a specific force of 0.6 newton-meters ( 5 in .-lbs.). There are several available pozidriv torquing screwdrivers.

## NOTE

When reinstalling or replacing one or both heater transistors (Q7 and Q8), replace both transistor insulators, HP Part Number 0340-0864. This is done to ensure the temperature stability of the oven crystal due to a balanced heat transfer to the oven mass from the heater transistors.

## 8-386. Special Test Connector

8-387. The following paragraphs describe a special connector, shown in Figure 8-8, fabricated for use in troubleshooting, alignment, and testing of the oven oscillator. The connector provides the following:
a. Two separate input leads for the power to the oscillator circuits and the oven heater/controller circuits.
b. $\mathbf{1 0 - M H z}$ output through a female BNC.
c. Oven monitor output for connection to a voltmeter.
d. EFC input connection to ground.


Figure 8-8. Special Test Connector

8-388. The following parts are required to construct the special test connector:
a. 15-pin pe board connector (HP Part Number 1251-0494).
b. 6 banana plugs (HP Part Number 1251-0124).
c. BNC female connector with ground lug and nut.

| BNC connector | $1250-0083$ |
| :--- | :--- |
| Ground lug | $0360-0024$ |
| Nut | $2950-0001$ |

d. Approximately 6 feet of 24 -gauge wire.
e. Labels for banana plugs.

8-389. To construct the connector:
a. Solder the center pin of the BNC connector to pin 1 of the printed circuit connector; this is the 10 MHz output signal.
b. Bend the BNC ground lug to align with pin 2 of the printed circuit connector.
c. Solder one end of a 2 -foot length of wire and the BNC ground lug to pin 2 of the printed circuit connector. This is the oscillator circuit common.
d. Solder one end of a 2 -foot length of wire to pin 3 of the printed circuit connector. This is the oscillator ( + ) supply.
e. Connect a jumper wire between pins 5 and 6 . This terminates the EFC input.
f. Solder one end of a 2 -foot length of wire to pin 11. This is the oven monitor output.
g. Solder one end of a 2 -foot length of wire to pin 14 of the printed circuit connector. This is the oven $(+)$ supply.
h. Solder one end of two 2 -foot lengths of wire to pin 15 of the printed circuit connector. This is the oven common.
i. Twist together one of the two wires connected to pin 15 and the wire connected to pin 14 . These are the oven controller power supply inputs.
j. Twist together the remaining wire connected to pin 15 and the wire connected to pin 11 . This is the oven monitor output.
k. Twist together the two wires connected to pins 2 and 3. These are the oscillator supply inputs.

1. Connect one banana plug to the free end of each wire.
m. Label each banana plug as follows:

Wire connected to:

## Label as:

pin 2
pin 3
pin 11
pin 14
pin 15 (two wires)
oscillator supply (-)
oscillator supply ( + )
oven monitor ( + )
oven supply (+)
oven monitor (-)
n. Inspect the connector for poor solder joints, bent, or damaged pins. Double check the labeling of the plugs to be sure the polarity markings are correct. If the voltages are connected the wrong way, damage to the oven oscillator may occur.

## 8-390. Types of Failures

8-391. Failures in the oscillator unit can be divided into two sections:
a. Failure of the oscillator's circuits.
b. Failure in the oven controller circuits.

8-392. Failures in the oscillator circuits can be divided into the following problems:
a. No output.
b. Output amplitude is too low or too high.
c. Output frequency is too low or too high.

8-393. Poor frequency stability can be difficult to troubleshoot and many times the oscillator is not at fault. Environmental conditions can affect stability and should be ruled out first.

8-394. Failures in the oven circuitry can be divided into the following problems:
a. No oven current (heat).
b. Excessive oven current ( $>600 \mathrm{~mA}$ ).
c. Oven does not cut back after warm-up (this will open the thermal fuse if allowed to continue).

8-395. Since the main oscillator and oven control power supply inputs are separate from each other, the defective circuit can be operated without applying power to the complete oscillator.

8-396. Determine which section is defective (oven or oscillator circuit), then proceed as described in the following troubleshooting section. The two circuits can be investigated separately.

## 8-397. Disassembly for Troubleshooting

$8-398$. To disassemble the oscillator unit:
a. Remove three screws securing bottom cover to outer housing, and remove bottom cover.
b. Remove two screws securing pc edge connector to outer housing.
c. Remove foam sheet to expose oven controller circuit board.

## CAUTION

With the cover and foam insulator removed, the thermal fuse cannot protect the oven circuit from thermal runaway. Caution should be used at all times.

If troubleshooting the oven controller, stop here and go to paragraph 8-400, Option 010 Oven Controller Troubleshooting. Go to Step d only if the trouble is in the oscillator circuit.

## WARNING

THE OSCILLATOR'S INTERNAL OVEN MASS TEMPERATURE MAY BE AS HIGH AS $85^{\circ} \mathrm{C}$ ( $185^{\circ} \mathrm{F}$ ). TO AVOID SERIOUS BURNS, DO NOT REMOVE OSCILLATOR CIRCUITS AND/OR OVEN MASS ASSEMBLY FROM THE OUTER CAN UNTIL THE OSCILLATOR HAS SUFFICIENTLY COOLED (APPROXIMATELY ONE HOUR WITH BOTTOM COVER AND FOAM INSULATOR REMOVED). THE OUTER HOUSING TEMPERAtURE IS NOT A RELIABLE INDICATION OF THE INTERNAL TEMPERATURE.
d. Using a long, small diameter tool, remove the complete oscillator assembly by inserting the tool into the tuning capacitor access hole (labeled FREQ. ADJ.) and gently pushing on the capacitor until the circuit can be grasped and removed easily.
e. Using a pozidriv screwdriver, remove two screws securing heater transistors to the oven mass. Remove washers and transistor insulators.

## NOTE

When reassembling the oven mass, the heater transistor screws must be tightened to a torque of 0.6 newton-meters ( 5 in .-Ibs.) (See paragraph 8385(c)).
f. Tilt oven oscillator assembly back and remove foam insulator between oven controller assembly and the oven mass. Be careful not to break the two black thermistor wires attached to the oven controller assembly.
g. Remove eight screws (four each side) securing the covers to the oven mass assembly.
h. Use two of the screws from each cover (removed in step g) to secure the boards to the oven mass for troubleshooting.

8-399. Go to paragraph 8-414, Option 010 Oscillator Circuit Troubleshooting. When reassembling unit, reverse the above procedure.

## 8-400. OPTION 010 OVEN CONTROLLER TROUBLESHOOTING

## 8-401. General

$8-402$. The oven controller section consists of three major circuits and a 10 V voltage reference for increased stability of sensitive circuits. Figure $8-9$ shows the major circuits and active components involved in their operation.

8-403. The temperature sense circuit monitors the temperature of the oven mass and reduces the power drawn by the oven heater transistors when the oven mass has reached operating temperature. After power cut-back, this circuit monitors the oven mass temperature and controls the power in the heaters to maintain the constant temperature. The thermistor (RT1) has a negative temperature coefficient. At room temperature the thermistor resistance is approximately $100 \mathrm{~K} \Omega$, while at operating temperature ( $\approx 82^{\circ} \mathrm{C}$ ) the resistance is approximately $9 \mathrm{~K} \Omega$. Shorting the thermistor to oven common makes the oven mass appear too hot to the temperature sense circuit. This in turn causes the temperature sense circuit to shut off power to the oven heaters. This technique is used in the troubleshooting procedure.

8-404. The warm-up current limit circuit controls the maximum current the oven may draw during warm-up ( 380 to 490 mA with 20 V dc oven input). This circuit is only active during the warm-up phase of the oven circuit operation.

## 8-405. Normal Operation

$8-406$. When the oven is tested under the normal conditions ( $\approx 25^{\circ} \mathrm{C}$ ambient temperature) it will initially draw 380 to 490 mA . After 5 to 10 minutes the oven current will start to drop. Over the next 10 to 15 minutes the oven current will fall to the 60 to 150 mA range where it will stabilize. The oven circuit should not oscillate.

## WARNING

> DO NOT OPERATE THE OVEN CIRCUITS WHEN THE OVEN MASS IS OUTSIDE OF THE OSCILLATOR INSULATED HOUSING. DOING SO WILL OVERHEAT THE OSCILLATOR CIRCUITS INSIDE THE OVEN MASS AND CAUSE PERMANENT DAMAGE. ALL OVEN TEST POINTS ARE AVAILABLE WITH THE OVEN MASS AND OVEN CONTROLLER CIRCUIT INSIDE THE HOUSING.
> WHEN OSCILLATOR COVER AND INSULATOR ARE REMOVED, THE THERMAL FUSE WILL NOT PROTECT CIRCUIT FROM OVERHEATING. APPLY OVEN POWER ONLY WHEN ACTUALLY MAKING MEASUREMENTS FOR TROUBLESHOOTING OR AS DIRECTED IN TROUBLESHOOTING TREE, FIGURE 8-10.

## 8-407. Troubleshooting Tree

8 -408. Figure 8 - 10 is a troubleshooting tree for the oven circuits. The troubleshooting procedure separates the different functional circuits by monitoring the oven supply current during different operating conditions. For example, if the warm-up current is excessive, this indicates a problem in the warm-up current limit circuit, or the current control and heater circuit. If shorting the thermistor reduces the current being drawn from the power supply, this indicates the current control circuit is operating and the problem is most likely in the warm-up current limit circuit.

8-409. As with most troubleshooting trees, this is intended to be a guide to the trouble area. It is not a substitute for technical skill in isolating the faulty components.

8-410. Table 8-11, Oven Circuit Voltages, gives normal circuit voltages during warm-up, operation, and when thermister RT1 is shorted to ground. Use this table during troubleshooting.

## 8-411. Troubleshooting Cautions

$8-412$. When oven current is excessive, turn on the power supply only long enough to make the necessary measurements. Do not leave power on if the oven is drawing excessive current. With the housing cover and foam insulator removed, the thermal fuse, F1, cannot protect the circuits in the oven mass from overheating and damage.

8-413. When power is applied to the oven controller circuit, it will go into its full warm-up mode. In this mode, the maximum heating power is applied to the oven mass. The oven mass is a metal casting surrounding the oscillator circuits and crystal. The OVEN MONTTOR output will be approximately 1.5 volts below the oven power supply voltage. In about 10 minutes, the oven will have heated to the proper temperature. The oven contoller will begin to regulate at this temperature and the OVEN MONTTOR will drop to approximately 3.5 volts. It is normal for the oven temperature to drop momentarily to a low value when the temperature first reaches maximum. This lasts less than a second and is a typical circuit action.


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Figure 8-9. Oven Controller Block Diagram

Table 8-11. Oven Circuit Voltages*

| VOLTAGE POINT | OVEN AT <br> OPERATING TEMP. | OVEN COLD (JUST <br> AFTER TURN-ON) | RT1 <br> GROUNDED |
| :---: | :---: | :---: | :---: |
| Q6B | 1.6 | 2.0 | 0.25 |
| Q6C | 11.4 | 11.4 | 11.4 |
| Q6E | 1.0 | 1.3 | 0 |
| Q7B | 12.5 | 12.7 | 11.9 |
| Q7C | 20.0 | 11.4 | 20.0 |
| Q7E | 11.4 | 11.4 |  |
|  |  | 1.3 | 0 |
| Q8B | 1.0 | 11.4 | 11.4 |
| Q8C | 0.07 | 0.23 | 0 |
| Q8E | 8.9 | 1.8 | 8.9 |
|  | 0.07 | 0.23 | 0 |
| U1 Pin 1 | 0.2 | 4.1 | 3.2 |
| U1 Pin 2 | 4.0 | 4.8 | 3.8 |
| U1 Pin 3 | 4.0 | 10.0 | 1.5 |
| U1 Pin 5 | 3.3 |  | 10.0 |
| U1 Pin 6 | 10.0 | 19.0 | 0.5 |
| U1 Pin 7 | 3.5 |  |  |
| U2 Pin 2 |  |  |  |
| U3 Pin 6 |  |  |  |

* Voltage readings taken with oven supply voltage of 20 V dc and insulating foam and cover removed.

Voltages are approximate and will vary slightly from unit to unit.


## 8-414. OPTION 010 OSCILLATOR CIRCUIT TROUBLESHOOTING

8-415. The oscillator circuits are relatively simple and straightforward. The following paragraphs will briefly describe the major circuit areas, a troubleshooting outline, and some helpful suggestions to make the troubleshooting process easier. The oscillator consists of four sections, listed below:
a. Oscillator $\mathrm{Q} 1, \mathrm{Q} 2$, and associated circuitry.
b. AGC Q3, CR4, CR5, and R6.
c. Output circuit Q5 and Q9.
d. 5.7 V power supply $\mathrm{CR} 2, \mathrm{CR} 3$, and Q 4 .

The oscillator is the signal source. Its output level is controlled by the AGC. The 5.7 V power supply provides an extra-stable clean voltage source for the oscillator circuits. The output circuits provide a high-level signal capable of driving a $50 \Omega$ to $1 \mathrm{~K} \Omega$ load.

## 8-416. Normal Operation

8-417. The output of the oscillator circuit at Q2 collector is a 10 MHz undistorted sine wave with an amplitude of approximately 2.8 V p-p. The AGC voltage (measured at CR5-C13 junction) is approximately -1.5 V . The 10 MHz signal passes through Q5 to Q9 base at about the same level. The voltage gain of amplifier Q5 (base to collector) is approximately 2 with a $50 \Omega$ load on the output. The output of transformer T 1 is approximately 1.5 V p-p. All 10 MHz signals found in the oscillator will be undistorted sine waves unless otherwise noted in Table 8-12, Oscillator Section Normal Voltages.

## 8-418. Troubleshooting

8-419. When troubleshooting the oscillator section, remove the oven mass from the housing and the covers from the oven mass as described in paragraph 8-397. Connect 12 V to the oscillator section; use the special connector described in paragraph 8-386, Special Test Connector. Set the power supply current limit to 60 mA . DO NOT apply power to the oven circuits!

8-420. Initial troubleshooting and probing should be done on the backside of the boards (trace side) while they are secured to the oven mass (see paragraph $8-398$, step $h$ ). This way the circuits are more easily handled. When the fault is isolated to a few components, the unit may then be disassembled for final troubleshooting and repair.

## 8-421. Helpful Hints

a. Most points in the oscillator circuits cannot be measured with a dc voltmeter. The reactance of the voltmeter probe and leads will load the circuit and give false readings. Instead, use an oscilloscope with a high input impedance probe for these measurements. Table 8-12, Oscillator Section Normal Voltages, indicates when a dc voltmeter can be used.
b. Before reinstalling the oven mass into the housing, adjust the output amplitude as instructed in paragraph 8-427, Output Amplitude Adjustment.

8-422. Symptoms of failures in the oscillator sections will generally fall into one of the following categories:
a. No output.
b. Output Amplitude is low or high.
c. Excessive drift of output frequency.

Table 8-12. Oscillator Section Normal Voltages
(see Notes 1, 2, 3)

| VOLTAGE POINT | NORMAL VOLTAGES |  | REMARKS |
| :---: | :---: | :---: | :---: |
|  | AC (p-p) | DC |  |
| C3/R3 | 1 to 4 |  | Note 8 |
| CR5/C13 |  | -1.5 | Notes 4 and 7 |
| CR3(C) | 0 | 6.3 | Note 4 |
| Q1(B) | 1 | 0.75 | Note 8 |
| Q1(C) | 0 | 5.5 | Note 4 |
| Q1(E) | 0.9 | 0.03 | Note 8 |
| Q2(B) | 0 | 2.7 | Note 4 |
| Q2(C) | 2.7 | 5.6 | Note 8 |
| Q2(E) | 0.06 | 2 | Notes 4 and 5 |
| Q3(B) | 2.7 | 5.6 | Note 8 |
| Q3(C) | 0 | 11.8 | Note 4 |
| Q3(E) | 2.4 | 4.9 | Notes 4 and 6 |
| Q4(B) | 0 | 6.3 | Note 4 |
| Q4(C) | 0 | 10.3 | Note 4 |
| Q4(E) | 0 | 5.6 | Note 4 |
| Q5(B) | 2.7 | 3.1 | Note 8 |
| Q5(C) | 0 | 11.8 | Notes 8 and 9 |
| Q5(E) | 2.8 | 2.6 | Note 8 |
| Q9(B) | 2.8 | 2.8 | Note 8, 9 |
| Q9(C) | 5.1 | 11.8 | Note 8, 9 |
| Q9(E) | 2.5 | 1.9 | Note 8 |
| NOTES |  |  |  |
| 1. All voltages taken with 12 V oscillator supply. |  |  |  |
| 2. Voltages are approximate and will vary slightly from unit-to-unit. |  |  |  |
| 3. All ac voltages are sine waves except Q2(E) and Q3(E). |  |  |  |
| 4. This dc voltage may be measured with a standard dc voltmeter. All other voltages should be measured with an oscilloscope and high impedance probe to minimize circuit loading. |  |  |  |
| 5. Waveform is $\quad$ um |  |  |  |
| 6. Waveform is slightly flattened on the bottom. |  |  |  |
| 7. This is the ACC voltage. Value shown is nominal with the oscillator operating. If the oscillator is not oscillating, the ACC voltage will be $\approx+2.5 \mathrm{~V}$. |  |  |  |
| 8. Measure both ac and dc voltages with an oscilloscope and a high impedance probe to minimize circuit loading. |  |  |  |

8-423. Troubleshooting of the faults listed in paragraph 8-422 is discussed in the following paragraphs.
8-424. NO OUTPUT. This is usually easy to repair by simple signal tracing. Localized fault finding (to actual defective component) can be somewhat more difficult if the problem is in the main oscillator circuit ( $\mathrm{Q} 1, \mathrm{Q} 2$, and AGC). If the fault appears to be the oscillator section and does not yield to normal troubleshooting tech-
niques, measure the AGC voltage at the junction of CR15-C13 (See Note 7 in Table 8-12, Oscillator Normal Voltages). If this voltage appears normal, the problem may be a defective quartz crystal (Y1). To verify this possibility, obtain a $10 \mu \mathrm{~h}$ (HP Part No. 9100-2265) and a $12 \mu \mathrm{~h}$ inductor (HP Part No. 9100-2242). (Use the HP numbered parts as these have been tested in the circuit.) On the oscillator board, remove the red and blue wires connecting the crystal to the board. Place the $12 \mu$ h inductor in place of these wires. With 12 V applied to the circuit. adjust the FREQ. ADJ. (C1) and the amplitude control (R6) for a good sine wave signal.

## NOTE

At some settings of C 1 and/or R6, intermittent oscillations may appear. Some minor adjustment of C 1 and/or R6 should clear this. If this fails, replace the $12 \mu \mathrm{~h}$ inductor with the $10 \mu \mathrm{~h}$ inductor and repeat the $\mathrm{C} 1 / \mathrm{R} 6$ adjustment.

8-425. If replacing the crystal with an inductor produces oscillation, this is a very good indication of a defective crystal. When replacing crystal Y1, read paragraph 8-384(b), Special Parts Replacement Considerations. If the circuit will still not oscillate, the problem is most likely one of the oscillator circuit elements.

8-426. OUTPUT AMPLITUDE HIGH OR LOW. Many times this can be cured by the adjustment of R6 as described in paragraph 8-427. If the correct amplitude cannot be obtained with this adjustment, monitor the signal at Q6 collector with an oscilloscope and set R6 to obtain an amplitude of 2.8 V p-p. Then check Q5 and Q9 stages. If the adjustment is not effective, investigate the operation of AGC circuitry (Q3, CR4, CR5, C5, C6, R5, R6, R7, or Q1).

## 8-427. Output Amplitude Adjustment

$8-428$. The output amplitude is adjusted by the setting of the variable resistor R6 which is in the feedback of the AGC circuitry. It is not accessible from the outside of the oscillator.

8-429. The following procedure should be used to adjust the output amplitude only if the output level falls outside the specified level, or repairs have been made to the main oscillator or AGC circuitry.
a. Remove oscillator from instrument.
b. Remove the three screws holding the bottom cover on the oscillator. Remove the bottom cover and allow the oscillator to cool (if previously operated).
c. Remove the two screws securing the P.C. edge connector to the outer can. Remove the top foam insulator to expose the oscillator circuits.

## WARNING

> THE OSCILLATOR'S INTERNAL OVEN MASS TEMPERATURE MAY BE AS HIGH AS $85^{\circ} \mathrm{C}$ (185 ${ }^{\circ}$ ). TO AVOID SERIOUS BURNS, DO NOT REMOVE OSCILLATOR CIRCUITS AND/OR OVEN MASS ASSEMBLY FROM THE OUTER HOUSING UNTIL THE OSCILLATOR HAS SUFFICIENTLY COOLED (APPROXIMATELY 1 HOUR WITH BOTTOM COVER AND FOAM INSULATOR REMOVED). THE OUTER HOUSING TEMPERATURE IS NOT A RELIABLE INDICATION OF THE INTERNAL TEMPERATURE.
d. Once the oscillator is cool enough to handle, remove the oscillator assembly by pushing on the tuning capacitor (FREQ. ADJ.) with a long, small diameter tool until the oscillator assembly can be removed easily.

## NOTE

Under no circumstances should the oven circuit be operated with the oven mass removed from the outer housing. To do so will cause damage to components inside the oven mass.
e. Required Equipment:
Oscilloscope.........................................HP 1715A (or equivalent)
Power Supply.........................................12V dc

Preset power supply to 12 V dc. Turn off power supply before proceeding to the next step.
f. Connect the power supply to pins $2(-)$ and $3(+)$ of the 15 pin test connector, as shown in Figure 8-11. (See instructions in paragraph 8-386, Special Test Connector, to fabricate the test connector.)

1. Insert the oscillator edge connector into the 15 pin test connector.
2. Connect pin 1 and 2 of the 15 pin test connector to an oscilloscope using a $50 \Omega$ coax cable. Set the oscilloscope to $50 \Omega$ input. Do not apply power to the oven circuits.
g. Turn on the power supply and adjust R6 AGC control for 1.56 V p-p $\pm 0.14 \mathrm{~V}$ p-p.
h. Turn off the power supply and reassemble the oscillator if the problem is corrected.

8-430. EXCESSIVE DRIFT OF OUTPUT FREQUENCY. When the quartz crystal oscillator has not been operated for a long period of time, or if it has been subjected to severe thermal or mechanical shock, the oscillator may take some time to stabilize. In most cases, the crystal will drift and then stabilize at or below the specified rate within a few days after being turned on. In isolated cases, depending on the amount of time the oscillator has been off and the environmental conditions it has experienced, the oscillator may take up to 1 week to reach the specified aging rate. This should be taken into consideration if the drift rate of the unit is out of
specifications. If the unit has had sufficient time to stabilize but is still out of specification, the most likely cause of excessive drift is a active crystal (Y1). If Y1 is to be replaced, read paragraph 8-384(b). Other possible causes are an unstable C3 and/or C8.

mona_l2
Figure 8-11. Output Amplitude Adjustment Setup

## 8-431. HP-IB BLOCK TROUBLESHOOTING

8-432. There are two Failure Messages from Table 3-4, in the Operating and Programming Manual, to help troubleshoot the HP-IB Block. Failure code 9.2 indicates that the HP-IB MCU is not responding and 9.4 warns of a communications failure between the Executive and HP-IB microcomputers.

8-433. To troubleshoot this block, first check all supply voltages, and also the TTL clock signal at pin 2 of MCU U17.

8-434. The HP-IB Operation Verification Test in Section IV of this manual can be used to verify proper operation of the HP-IB Block. Refer to Section IV, paragraph 4-41, for details.

8-435. If the HP-IB Verification Test will not run, use the HP-IB test setup from Section IV and the following instructions to help troubleshoot a failure.

8-436. Check to see if the REMOTE ENABLE and INTERFACE CLEAR latches are setting and clearing properly.
a. When the REN (REMOTE ENABLE) line of the HP-IB bus goes HIGH (U10 pin 11), the REN latch goes LOW (U8 pin 11) and the HP-IB MCU tries to clear the latch.

1. To force the REN line (U10 pin 11 and 12) HIGH, send the HP-IB command: LOCAL 7

BASIC Program:
10 REMOTE 7
20 LOCAL 7
30 END

RUN
2. To force the REN line LOW, send the HP-IB command: REMOTE 7

BASIC Program:
10 LOCAL 7
20 REMOTE 7
30 END

RUN
b. When the IFC (INTERFACE CLEAR) latch output at U8 pin 6 goes LOW, the HP-IB MCU tries to clear the latch.

To check the IFC line (U8 pin 1), use the following program.
BASIC Program:
10 ABORTIO 7
20 GOTO 10

RUN

This program outputs pulses on the IFC line of the HP-IB bus. The latch should output the same pulses at U8 pin 6 except when the latch output is LOW, the HP-IB MCU tries to clear the latch which causes the output to go HIGH momentarily.
c. The ATN (ATTENTION) line and the discrete gates of U9 can be checked using the following statements:

1. To force the ATN line LOW, send the HP-IB command: SEND 7; CMD 0

BASIC Program:
10 SEND 7; CMD 0
20 END

RUN
When the ATN line (U9 pin 1 and 2) goes LOW, pin 25 of the HP-IB MCU should go HIGH and the MCU should drive pin 9 of U9 LOW. Also, the HP-IB MCU will output a LOW to pin 9 of U6.
2. To force the ATN line HIGH, send the HP-IB command: RESET 7

BASIC Program:
10 RESET 7
20 END

RUN
When the ATN line (U9 pin 1 and 2) goes HIGH, pin 25 of the HP-IB MCU should go LOW and the MCU should drive pin 9 of U9 HIGH. Also, the HP-IB MCU will output a HIGH to pin 9 of U6.
d. Transceiver IC U6, which drives the HP-IB DATA lines can be checked for Output using Signature Analysis (Refer to the Signature Analysis Troubleshooting section which follows Signal Tracing.)

To check U6 data lines for Input, use the following statements:
BASIC Program:
10 SEND 7; CMD 85
20 SEND 7; CMD 170
30 GOTO 10

RUN
Check that all of the data lines toggle and the inputs match the outputs.
e. Transceiver IC U7 may be checked with the following program:

## NOTE

This test requires an input signal to the Counter. Connect the Time Base output from the rear panel of the Counter to Input A.

The following program makes use of all the lines on U7. Check that the inputs match the outputs, and that the signals on pins $1,7,9$, and 15 change state.

```
BASIC Program:
    10 CONTROL 7, 16; 129, 13, }1
    20 OUTPUT 703; "IN, FN1, GA.001, HS1"
    30 ENTER 703 USING "%, %K"; X$
    40 GOTO 20
    50 END
    RUN
```

8-437. Signature Analysis can be used to help troubleshoot the HP-IB Block. The instructions for using Signature Analysis to troubleshoot the HP-IB Block starts in paragraph 8-456, Signature Analysis.

## 8-438. OPTION 030 CHANNEL C TROUBLESHOOTING

8-439. The Channel C Input Amplifier Block consists of the following circuits: input signal conditioning, amplifier, prescaler, peak detector/threshold comparator, and buffer. Refer to Figure 8-26, Channel C Input Amplifier Block Schematic Diagram.

8-440. The output (U303 pin 1) of the three-stage Amplifier drives the Divider (U302) and Peak Detector (CR302). The Peak Detector sends a signal to the Threshold Comparator (U306) that gates the output of the Divider through the output Buffer (U301) to the rest of Counter. (The gating technique is used to prevent the Counter from counting the random numbers that the Divider naturally produces, when the Divider has an insufficient input signal.)

## NOTE

The Peak Detector circuit consists of two major active components: the Peak Detector diode CR302 and Threshold Comparator U306, which is the output of the Peak Detector circuit. Thus, throughout the remainder of this troubleshooting procedure any mention of "Peak Detector" is referring to both the Peak Detector CR302 and Threshold Comparator U306 and their associated components.

## 8-441. Determining the Failed Circuit in the Channel C Block

8-442. To troubleshoot the Channel C Block, you must determine which of the following three categories the problem falls into:

- The Peak Detector does not enable the Divider, resulting in no output at pin 4 of U302 (Divider).
- The Peak Detector properly enables the Divider, but the output of Divider (Pin 4 of U302) is incorrect or non-existent.
- The Peak Detector improperly enables the Divider. The Counter works properly with a signal applied to Channel C, but it randomly counts when the signal is removed from the Channel C input.
8-443. The following procedure will help determine which category a failure falls into. Note that U306 pin 1 is the output of the Peak Detector. When pin 1 is at $-1.2 \mathrm{~V} \pm 0.4 \mathrm{~V}$, the Peak Detector enables the Divider; and when pin 1 is at $-5 \mathrm{~V} \pm 0.4 \mathrm{~V}$, the Peak Detector disables the Divider.

8-444. The flowchart in Figure 8-12, simplifies the Channel C troubleshooting procedures.


Figure 8-12. Channel C Troubleshooting Flowchart
a. Connect the HP 8656B Signal Generator RF OUTPUT to INPUT C of the HP 5334B. Set up the HP 8656B and HP 5334B as follows:

HP 5334B
FREQ C....................................................ON
HP 8656B
Frequency................................................... 90
Amplitude .................................................. 30 dBm
b. Using an oscilloscope or digital voltmeter, check for $1.2 \mathrm{~V} \pm 0.4 \mathrm{~V}$ at pin 1 of U 306 . If $-1.2 \mathrm{~V} \pm 0.4 \mathrm{~V}$ is present at pin 1 , perform step $c$. However, if $-1.2 \mathrm{~V} \pm 0.4 \mathrm{~V}$ is not present at pin 1 , perform the following steps:

1. Perform the procedure in paragraph $8-445$, Troubleshooting the 30 dB Amplifier Circuit.
2. If the RF signal was not present in the previous step (1) the Peak Detector circuit is suspected; thus, perform the procedures in paragraph 8-449, Troubleshooting of the Peak Detector Circuit.
c. Remove the signal from INPUT C and observe $-5.0 \mathrm{~V} \pm 0.4 \mathrm{~V}$ at pin 1 of U 306 . Now, read and perform, if necessary, the following steps:
3. When $-5.0 \mathrm{~V} \pm 0.4 \mathrm{~V}$ is present at U 306 pin 1 , the Peak Detector is working properly, but a problem that is causing an incorrect count might exist in the Divider circuit. If this is the case, perform procedure in paragraph 8-447, Troubleshooting the Divider circuit.
4. If $-1.2 \mathrm{~V} \pm 0.4 \mathrm{~V}$ is present at U 306 pin 1 , the Threshold Comparator is always enabling the Divider circuit. Note that HP 5334B displays a random count. If this is the case, perform the procedure in in paragraph 8-454, Troubleshooting the Threshold Comparator.
d. Repeat steps a through c with HP 8656 A set to output a 990 MHz signal.

## 8-445. Troubleshooting the $\mathbf{3 0} \mathbf{d B}$ Amplifier Circuit

8-446. The input signal is received through the INPUT C connector and routed to the Channel C Input Block where it is coupled, attenuated, and fed to pin 3 of U305 (the first stage of the 30 dB Amplifier) and through U304, and U303. The output of the amplifier is then fed to the Peak Detector and Divider. To troubleshoot the amplifier chain perform the following:
a. With no signal applied to Channel C, check for a dc bias of 4 to 6 volts at pin 1 of U303, U304, and U305. (Pin 1 is the output and is the square pad located at the rear of the amplifier.)

1. If an output is lower than 4 Vdc , the pull-up resistors for the particular output are suspected.
2. If an output is at zero volts, check for a short to ground. If the outputs are not shorted to ground then perform the next step, $b$.
b. Check the input voltage at each of the amplifiers (U303, U304, and U305) at pin 3 for a 1.6 volts dc level. If you measured a different voltage at any of the inputs, the pull-up resistors for the particular input are suspected.
c. Connect a 90 MHz signal at -10 dBm to INPUT C.
d. Now, using an HP 8565A Spectrum Analyzer, trace the signal through the amplifier chain to find where the signal drops out.

## Set up the HP 8565A Spectrum Analyzer as follows:

## FREQUENCY SPAN/DIV

FREQUENCY BAND $0.01-1.8 \mathrm{GHz}$
FREQUENCY SPAN MODE. ..... PER DIV
FREQUENCY SPAN/DIV. ..... 500 KHz
RESOLUTION BW ..... 10 KHz
REFERENCE LEVEL/INPUT ATTEN
REFERENCE LEVEL ..... 0 dBm
INPUT ATTEN .....
AMPLITUDE SCALE ..... 10 dB
SWEEP TRIGGER ..... FREE RUN
SWEEP SOURCE ..... INT
e. Check for the following signal peaks at 90 MHz :

U303 pin $1-65 \mathrm{dBm}$
U304 pin $1-70 \mathrm{dBm}$
U305 pin $1-75 \mathrm{dBm}$
f. Now, set the Spectrum Analyzers FREQUENCY SPAN to 0.990 GHz .
g. Set the HP 8656 B Signal Generator to output a 990 MHz signal to INPUT C.
h. Check for the following signal peaks at 990 MHz :

U303 pin $1-65 \mathrm{dBm}$
U304 pin $1-75 \mathrm{dBm}$
U305 pin $1-85 \mathrm{dBm}$
i. If all the dc checks and signal tracing are good, then the 30 dB Amplifier circuit is good.

## 8-447. Troubleshooting the Divider Circuit

8-448. Divider U302 divides the input signal by 64. The Divider is more sensitive than the Peak Detector. Thus, once you supply enough input signal to turn on the Peak Detector, the Divider circuit should operate.
a. Connect the $90 \mathrm{MHz},-30 \mathrm{dBm}$ signal to INPUT C.
b. Check the dc bias of U302 pin 1 and U302 pin 8 . There should be -2.6 V at both pins.
c. Verify that there is a $1.4 \mathrm{MHz}, 1.5 \mathrm{Vp}-\mathrm{p}$ square wave with -2.6 V dc offset at U 302 pin 4.
d. Verify the pins 2,3 , and 6 are grounded. Note that if for some reason pins 3 or 6 lost their connection to ground, they will float down to $-5.0 \mathrm{~V} \pm 0.4 \mathrm{~V}$ and cause the prescaler to divide by 128 or 256 , instead of by 64 .
e. If all of the above dc levels were correct, then the problem may be with bias resistor R304, or U301. U301 might not be sending its signal to MRC U20. Verify that R304 is biasing U301 pin 5 to -1.2 V $\pm 0.4 \mathrm{~V}$ and that the output, U301 pin 3, is not shorted or pull-down by resistor R302.
f. Check for a 400 mV p-p square wave with +2.6 V dc offset at U 301 pin 3. This is the output of the Channel C Input Amplifier and it is sent to MRC U20, which is located in the Measurement Block. Thus, if Channel C Input Amplifier is working, perform the troubleshooting procedures in paragraph 8-358, Measurement Block Troubleshooting.

## 8-449. Troubleshooting the Peak Detector Circuit

8-450. The purpose of the Peak Detector circuit is to sense when an input signal is present or not present. When an input signal is present, the Peak Detector enables the HP 5334B to count, and when no (or insufficient) input signal is present, it disables counting.

## 8-451. TROUBLESHOOTING THE PEAK DETECTOR DIODE

8-452. When the Peak Detector goes bad, the most common symptom is that the signal going to the comparator (U306-2) will have a large offset voltage. To troubleshoot the Peak Detector, perform the following:
a. Remove signal from INPUT C.
b. Check for a voltage of about +0.2 V at the junction of the Peak Detector diode CR302 and resistor R309.
c. Check for a voltage of about -0.2 V at the junction of the CR302 and resistor R308.
d. If you measured 0 V at either of the junctions in the previous steps, $b$ and $c$, check the node(s) for shorts to ground.
e. If there is no obvious shorts, unsolder CR302 and remove it form the the circuit board.
f. Using a ohmmeter, measure for shorts in CR302. If CR302 checks out good, then check the bias current circuits in the following step.
g. Check for about +0.7 V at the anode of CR304 and for 0.7 V at the cathode of CR305.
h. If all the above checks are good, replace CR302.

## 8-453. TROUBLESHOOTING THE THRESHOLD COMPARATOR

8-454. Comparator U306 output (pin 1) depends on the relationship of its two inputs; that is, when the voltage at pin 2 is less (more negative) than the voltage at pin 3 , pin 1 should be at $-1.2 \mathrm{~V} \pm 0.4 \mathrm{~V}$. When the voltage at pin 2 is more (less negative) than the voltage at pin 3 , pin 1 should be at $-5.0 \mathrm{~V} \pm 0.4 \mathrm{~V}$.

8-455. To determine if the Threshold Comparator circuit is functioning properly, perform the following:
a. Connect a $90 \mathrm{MHz},-30 \mathrm{dBM}$ signal to INPUT C.

## CAUTION

If your HP 5334B contains a Revision A, B, or C A1 Main Board, read the the following instruction:

To prevent shorting out resistor R319, you must not leave potentiometer R328 (Threshold Adjust) in its fully clockwise position too long.
b. Adjust R328 so that the voltage at U306 pin 2 is less (more negative) than the voltage at U306 pin 3.
c. Verify that U 306 pin 1 is $-1.2 \mathrm{~V} \pm 0.4 \mathrm{~V}$. If the voltage at pin 1 is not $-1.2 \mathrm{~V} \pm 0.4 \mathrm{~V}$, the comparator circuit is malfunctioning; go to step $f$.
d. Adjust potentiometer so that pin 3 is less (more negative) than pin 2.
e. Verify that pin 1 is $-5.0 \mathrm{~V} \pm 0.4 \mathrm{~V}$. If the voltage at pin 1 is not $-5.0 \mathrm{~V} \pm 0.4 \mathrm{~V}$, the comparator circuit is malfunctioning; go to step f .
f. Replace U306. After replacing U306 and a problem still exists in the Threshold Comparator circuit, check R328 and the other components (such as R319, R318, C324, and C329) connected to U306; they could be preventing U306 from working properly.
g. Check bias resistor R303 and ECL Buffer U301 pin 11.

## 8-456. SIGNATURE ANALYSIS

8-457. Signature Analysis can be used to troubleshoot the 5334B. Correct signatures are defined as the signatures documented in the troubleshooting procedure of the 5334B. An incorrect signature is defined as a signature displayed on the signature analyzer that does not match the documented one for the node being probed. If the correct signatures are repeatable, then measuring an incorrect signature during troubleshooting will accurately indicate an incorrect waveform for that node. The troubleshooter can then quickly back-trace through the circuit following incorrect waveforms to the faulty node. The fault is found at the point where back-tracing further results in correct signatures. For instance, if the signature for an output of a device is incorrect, signatures are taken at the inputs for that device. If the input signatures are correct, then the fault has been isolated to the output node. If any input signature is incorrect, back-tracing continues along that signal path.

## NOTE

The signatures listed in this manual are intended to apply only to instruments with serial number prefixes up to and including those called out on the title page. Newer instruments will have a Manual Change Supplement supplied with the manual to note differences (if any) with the published signatures.

8-458. The Signature Analysis testing is designed so that the Executive and HP-IB microcomputers (MCUs) can be tested separately from the rest of the instrument. The connection instructions are included for the two MCUs in the following paragraphs.

## 8-459. Executive and HP-IB Block Signature Analysis Troubleshooting

8-460. Signature Analysis can be used to troubleshoot the Executive and HP-IB Block components. Follow the instructions given below.

## Setup:

a. Begin with the 5334B in STANDBY.
b. Connect a jumper between the Executive MCU (U19) ST or SP pin (TP17 or TP18) and Ground (TP8).
c. Connect a jumper between the HP-IB MCU (U17) ST or SP pin (TP14 or TP 15) and Ground (TP8).
d. Apply power to the 5334B and observe that the Counter displays "SA dIAG".
e. Remove jumpers from ST/SP and Ground for both MCUs.

## NOTE

The 5334B must remain ON and displaying "SA diAG".
f. To check the EXECUTIVE BLOCK using Signature Analysis, connect Pod Leads from the signature analyzer to the A1 Main Board as follows:

| Signature Analyzer | U19 Test Points |
| :--- | :--- |
| START LEAD | ST (TP17) |
| STOP LEAD | SP (TP18) |
| CLOCK LEAD | SA CLK (TP13) |
| GROUND LEAD | Ground (TP8) |

1. Apply power to the signature analyzer and observe that its GATE light is flashing.
2. Set the signature analyzer push button switches as follows:

START BUTTON
Rising Edge
STOP BUTTON
Falling Edge
CLOCK BUTTON
Falling Edge
3. Take signatures. Signatures should match those shown in Figure 8-13.


Figure 8-13. Executive Block Signatures
g. To check the HP-IB BLOCK using Signature Analysis, connect Pod Leads from the signature analyzer to the A1 Main Board as follows:

| Signature Analyzer | Ui7 Test Points |
| :--- | :--- |
| START LEAD | ST (TP14) |
| STOP LEAD | SP (TP15) |
| CLOCK LEAD | SA CLK (TP16) |
| GROUND LEAD | Ground (TP8) |

1. Apply power to the signature analyzer and observe that its GATE light is flashing.
2. Set the signature analyzer pushbutton switches as follows:

| START BUTTON | Rising Edge |
| :--- | :--- |
| STOP BUTTON | Falling Edge |
| CLOCK BUTTON | Falling Edge |

3. Take signatures. Signatures should match those shown in Figure 8-14.


Figure 8-14. HP-IB Block Signatures

## 8-461. OPTION 700 MATE BLOCK TROUBLESHOOTING

8-462. Troubleshooting procedures for the MATE Block are divided into two parts. The first employs the self checking operation of the Counter and basic signal testing with a voltmeter and an oscilloscope. The second troubleshooting method uses signature analysis, described in paragraph 8-451. This is the primary technique for troubleshooting the MATE Block.

8-463. MATE failures prevent the remote control operation of the HP 5334B, Option 700 Counter. The Counter's proper operation in the local mode is unaffected.

## WARNING

Maintenance described in this section is performed with power supplied to the instrument and protective covers removed. This maintenance should be performed only by qualified service personnel who are aware of the hazards involved (for example, fire and electrical shock). Where maintenance can be performed without power applied, the instrument should be disconnected from its power source.

## 8-464. Self-Test and Basic Signal Checking

a. When the HP 5334B is switched ON, it performs a self-test to verify the operation of its various subsections. If a FAIL 9.2 or a FAIL 9.4 message is displayed, the MATE Block could possibly be faulty. This failure can be verified by isolating the MATE Block from the instrument. Skip to step dif you do not want to isolate the MATE Block.
b. MATE BLOCK ISOLATION:

1. Turn power OFF.
2. Remove integrated circuits U702, U704, U705, and U706 from their sockets on the A1 Main Board.
3. Insert a 16 pin jumper chip (HP Part Number 1251-4787) in the U705 and U706 designations on A1 Main Board. Place the jumper chip in such a way that pins $1,10,11$, and 20 are not jumpered, as shown in the following illustration:

## Jumper Configuration for Sockets XU705 and XU706

10 ..... 020
20 ..... 19
30 ..... 18
40 ..... 17
5 ..... 16
60 ..... 15
7 ..... 14
80 ..... 13
90 ..... 12
100 ..... 011
4. Insert three jumpers (or 0 ohms resistors) in the R271, R272, and R273 designations, located in the U702 designation (see Figure 8-19. HP 5334B Component Locator).
5. Short together "CLK" signal to "GND" (ground) by placing a jumper wire between pins 7 and 9 of $\mathbf{J 7 0 1}$.
c. Switch ON the HP 5334B. If the failure message does not appear, then you know the failure is in the MATE Block; therefore, continue with the the following troubleshooting steps.
d. Verify that the following power supplies are within the specified range on the MATE Block:

| Supply | Test Point | Range |
| :--- | :--- | :---: |
| +5 V | $\mathrm{~J} 701(1)$ | +4.8 V to +5.2 V |
| $+5 \mathrm{~V}(\mathrm{~F})$ | $\mathrm{U708}(28)$ | +4.8 V to +5.2 V |
| +5 V at U2 | U702 (7) | +4.8 V to +5.2 V |

e. Verify the following signal levels in the MATE Block:

- The reset signal (J701 pin 8) should switch from a low to high level between 100 and 200 ms after the power supply reaches +4.8 V from power off.
- The NMI signal (U702 pin 4) should be at a TTL high.
- The IRQ1 signal (J701 pin 10) should be at a TTL high.
- The clock signal (J701 pin 7) should be a 1 MHz TTL square wave.

These signals should be correct before continuing with the signature analysis troubleshooting.

## 8-465. MATE Block Signature Analysis Troubleshooting

8-466. Perform the troubleshooting steps below after checking the Counter's operation with the "Self-Test and Basic Signal Checking" procedures of paragraph 8-464.

8-467. The HP 5334B, Option 700 has three setups for signature analysis. Each setup uses a different signal for the signature analyzer CLOCK input. The three setups should be performed in sequence.

## 8-468. SIGNATURE ANALYSIS SETUP \#1

To perform signature analysis for Setup \#1, proceed as follows:
a. Switch OFF power to the Counter.
b. Remove U704 from its socket.
c. Attach the test pod leads of the signature analyzer as follows:

ST/SP//START: J701, pin 6
QUAL/STOP: J701, pin 1 (VCC)
CLOCK: U702, pin 39
GND: J701, pin 9 (GND)
d. Set the signature analyzer as follows:

FUNCTION: QUAL
CLOCK: falling edge
START: rising edge
STOP: rising edge
QUAL: high level
e. Power up the Counter and verify the signatures shown in Figure 8-15.

|  | *OOOT |  |
| :---: | :---: | :---: |
|  |  | * = PROBE LED FLASHING <br> $x=D O N^{\prime} T$ CARE |

Figure 8-15. HP 5334B, Option 700 Signatures for Setup 1

## 8-469. SIGNATURE ANALYSIS SETUP \#2

To perform signature analysis for Setup \#2, proceed as follows:
a. Switch off power to the Counter.
b. Attach the test pod leads of the signature analyzer as follows:

ST/SP//START: J701, pin 6
QUAL/STOP: J701, pin 1 (VCC)
CLOCK: J701, pin 7 (CLK)
GND: J701, pin 9 (GND)
c. Set the signature analyzer as follows:

FUNCTION: QUAL
CLOCK: falling edge
START: rising edge
STOP: rising edge
QUAL: high level
d. Power up the Counter and verify the signatures shown in Figure 8-16.


Figure 8-16. HP 5334B, Option 700 Signatures for Setup 2

|  |  |  |
| :---: | :---: | :---: |
|  |  |  |
|  | ```* = PROBE LED FLASHING X = DON'T CARE``` |  |

Figure 8-16. HP 5334B, Option 700 Signatures for Setup 2
(Continued)

## 8-470. SIGNATURE ANALYSIS SETUP \#3

8-471. To perform signature analysis for Setup \#3, proceed as follows:
a. Switch off power to the Counter.
b. Attach the test pod leads of the signature analyzer as follows:

ST/SP//START: J701, pin 6
QUAL//STOP: U709, pin 22
CLOCK: J701, pin 7 (CLK)
GND: J701, pin 9 (GND)
c. Set the signature analyzer as follows:

FUNCTION: QUAL
CLOCK: falling edge
START: rising edge
STOP: rising edge
QUAL: low level
d. Power up the Counter and verify the signatures shown in Figure 8-17.


Figure 8-17. HP 5334B, Option 700 Signatures for Setup 3

## 8-472. MATE SIGNATURE ANALYSIS SUMMARY

8-473. There are three active components in the MATE Block that are not fully diagnosed by signature analysis. They are the microprocessor, U2, the RAM, U8, and the EPROM, U9. Should signature analysis fail to detect a problem on a known bad board, these three components should be replaced, one at a time.

8-474. When signature analysis troubleshooting is completed, switch off power to the Counter, return U704 to its socket, and plug the W1 cable back into the main board J15 connector.

This completes the troubleshooting procedures for the MATE Block.

## 8-475. FIELD INSTALLATION OF OPTION 010

8.476. Only Option 010 Oven Oscillator is available for field installation.

8-477. To obtain the necessary parts for installation of Option 010, order by part number as listed in Section VI. Contact the nearest HP sales office listed at the end of the manual if there are any questions about parts ordering or option installation.

8-478. In the following installation procedure, it is assumed that an instrument is currently without the option being installed.

## CAUTION

Static electricity can result in permanent degradation or catastrophic failure of the instrument or assemblies removed from the instrument. All work performed on instruments, or on assemblies, must be at static-safe work stations providing proper grounding for the operator.

## NOTE

Whenever using a wrench on the front panel, be careful not to scratch the paint by turning the wrench while it is is against the panel.

8-479. Obtain the ovenized oscillator (10811-60111), and two screws (2360-0129) as listed in the Option 010 portion of Table 6-2 Replaceable Parts on page 6-18.

8-480. Tools Required:
Pozidriv Screwdriver
Large Pozidriv Screwdriver

## NOTE

Refer to the exploded view in Figure 6-1 when performing this field installation procedure.

8-481. Install Option 010 as follows:
a. Disconnect the power cable from the HP 5334B.
b. On the rear panel of the instrument, remove the bumper feet (MP4, 4040-1991), using the Pozidriv screwdriver.
c. Remove screw (0515-0886) that secures the cover to the rear panel.
d. Using the large Pozidriv screwdriver, remove the two screws ( $0515-1132$ ) on both sides of the cover. The right side (viewing the 5334B from the rear panel) has a handle; therefore, removing these two screws will enable you to remove the handle.
e. Now, slide the cover off the instrument's chassis.
f. Plug the Oven oscillator into the edge connector J204 located on the left side of the Main board (viewing from the rear panel).
g. Secure the oven oscillator with two screws (HP Part Number 2360-0129). Insert the screws through the standoffs and tighten; and perform the following steps (refer to A1 Main Board Component Locator, Figure 8-19):

1. Remove 10 MHz crystal oscillator (Y1).
2. Unsolder and remove capacitor C8 (keep C8 for reuse in step 4).
3. Clear solder holes at $\mathbf{C} 100$ designation.
4. Install C8 into C 100 designation and solder.
5. Now, power the 5334B ON. Leave power ON for at least 20 minutes to allow the oven oscillator to warm up.
6. After 20 minutes warmup, calibrate per specifications.
h. Finally, reinstall the cover, handle, and rear panel feet by performing the following steps:
7. With rear of the instrument facing you, attach the cover to chassis. Place as far to front frame as is possible. Line up the holes for the bumper feet on the rear.
8. With right side (viewing from rear) up, lay strap handle assembly (MP14, 05060-9802) along the center groove of side of top cover.
9. Place front handle cap (MP12, 5041-6819) over strap handle on end toward front frame. Hand start screw.
10. Place rear handle cap, J shaped, (MP13, 5041-6820) over strap handle on the end toward the rear of instrument. Hand start screw.
11. Tighten both screws using the large Pozidriv screwdriver.
12. On opposite side, secure cover by tighting the two screws.
13. Place bumper feet on rear of instrument, curved side facing away from instrument. Tighten screws for both feet.
(This page intentionally left blank)

Figure 8-18
OVERALL BLOCK DIAGRAM



Figure 8-20 P/O A1 MAIN BOARD INPUT AMPLIFIER BLOCK SCHEMATIC DIAGRAM (Sheet 1 of 7 )
(See Page 8-95)





##   

 $A$ descripption of he sussel al min boafo asserblies


Taple of Active elenevis






Figure 8-22 P/O AI MAIN BOARD EXECUTIVE/MEASUREMENT BLOCK SCHEMATIC DIAGRAM (Sheet 3 of 7 )

P/O A1 ASSEMBLY EXECUTIVE/MEASUREMENT BLOCK



Figure 8-23
P/O A1 MAIN BOARD HP-IB BLOCK
SCHEMATIC DIAGRAM (Sheet 4 of 7 )


P/O Figure 8-23. A1 HP-IB Block





3. ASERISK (*) INDINATES FACTOPY
 . circuit notes:
$\left.\begin{array}{c}\text { sotroan view } \\ 0 . \\ o \quad \\ 0 \\ 0 \\ 0\end{array}\right]$
6. 1/4 of U10(U16C) is on SHEET
7. ${ }^{\nabla}$ Instrement common.








Figure 8-24


P/O Figure 8-24. A1 Timebase/Power Supply Blocks



2. UNLESS OTHEFWISE INOICATED:


4. ATHDE (**) Pregeong in in
circuit notes

| $\mathrm{E}=\mathrm{BC}$ |
| :---: |
| 000 |

6. AN INSTRRMENT WITHA STANARD OSGILLTOR

7. EARTH GROUND is connected to standoff on


| table of active elments |  |  |
| :---: | :---: | :---: |
| Referice | art no. | nfg part no. |
|  | 1992 |  |
| ${ }_{\text {cose }}^{\text {cata }}$ | 1992-8959 | Same |
| cicterein |  | ${ }^{\text {P22 }}$ |
| crear | - | Poze |
| ${ }_{\text {U11 }}$ | 1828-9889 | Mc1611 |
|  |  |  |
|  | (182-9333 | Mc7965. zct |
| (2095 |  |  |



 | DESIGNATOR | + SV | ono |
| :---: | :---: | :---: |
| U11 | 1,16 | 8 |



P/O Figure 8-25. A1 Option 700 MATE Block


P/O A1 ASSEMBLY OPTION O3O CHANNEL C BLOCK


NOTE
There is no actual connector at J302. Cable W2 is soldered directly to the board in the installation of Opt. 060.

notes


2. UNLESS OTHEEYTIERERITITITCATEO:




7. $-1.2 v$ WHEN CoNTTNG:






 | U381 |  | 11 |  | 8 |
| :--- | :--- | :--- | :--- | :--- |
| U382 |  |  | 5 | 2.3 .6 |
| U383 | 1 |  |  | 2.4 |
| U334 | 1 |  |  | 2.4 |
| U385 | 1 |  |  | 2.4 |
| U386 | 8 |  |  | 4 |

Figure 8-27


OPTION OIO OVEN OSCILLATOR BLOCK SUPPLY BLOCKS SCHEMATIC DIAGRaM.



Figure 8-28
A2 FRONT PANEL BOARD SCHEMATIC DIAGRAM




[^0]:    HP 5334B - Service Manual 5-20

